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IP Block Datasheet Template V0.0

Designer's name

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Disclaimer

Design status	Main designer	Contact person
Work in progress Silicon proven Irradiated	Designer's name	Contact person (contact.person@cern.ch)

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Contents

1 Introduction

This document summarizes the specifications and reviews the architecture of the **IP block** designed in TSMC 28 nm (N28HPC+) technology.

The reported values in this document are preliminary (based on schematic-level and extracted simulations).

2 General Description

Figure 1 shows how to place and reference a figure. And this is how you make a citation [1].

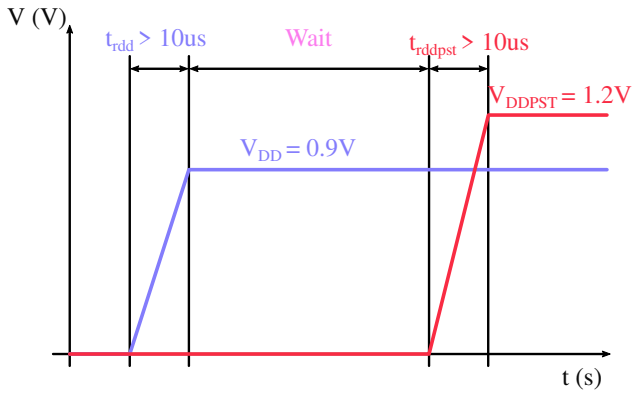

Figure 1: Example.

References

[1] S. Kulis, "Single Event Effects mitigation with TMRG tool," *Journal of Instrumentation*, vol. 12, no. 01, p. C01082, 2017. [Online]. Available: http://stacks.iop.org/1748-0221/12/i=01/a=C01082