

VOLTUS-FI

EMIR PVS Flow
Step-by-Step

by

Rui Francisco

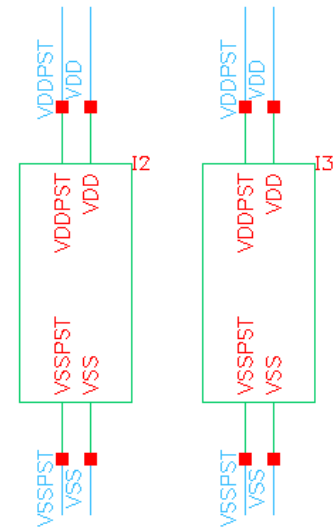
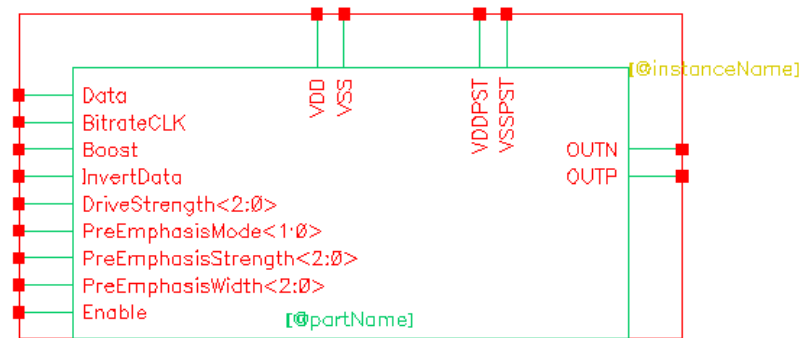
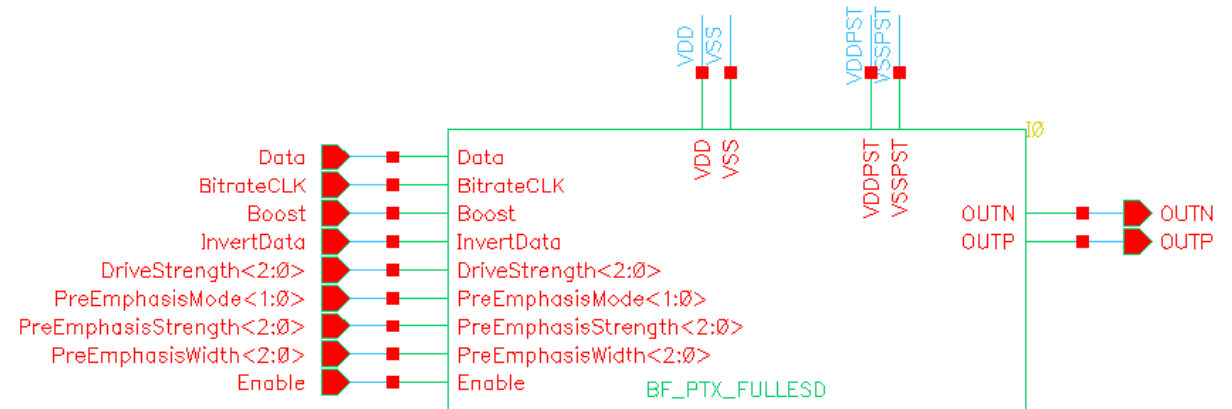
rui.francisco@cern.ch

Requirements

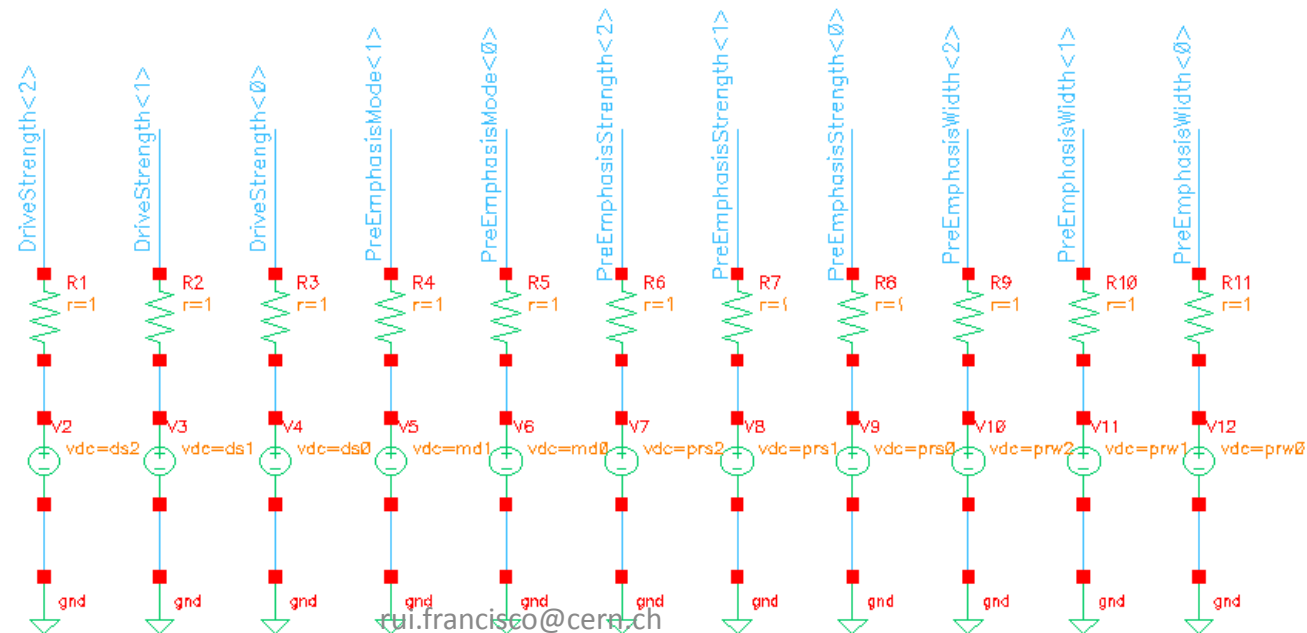
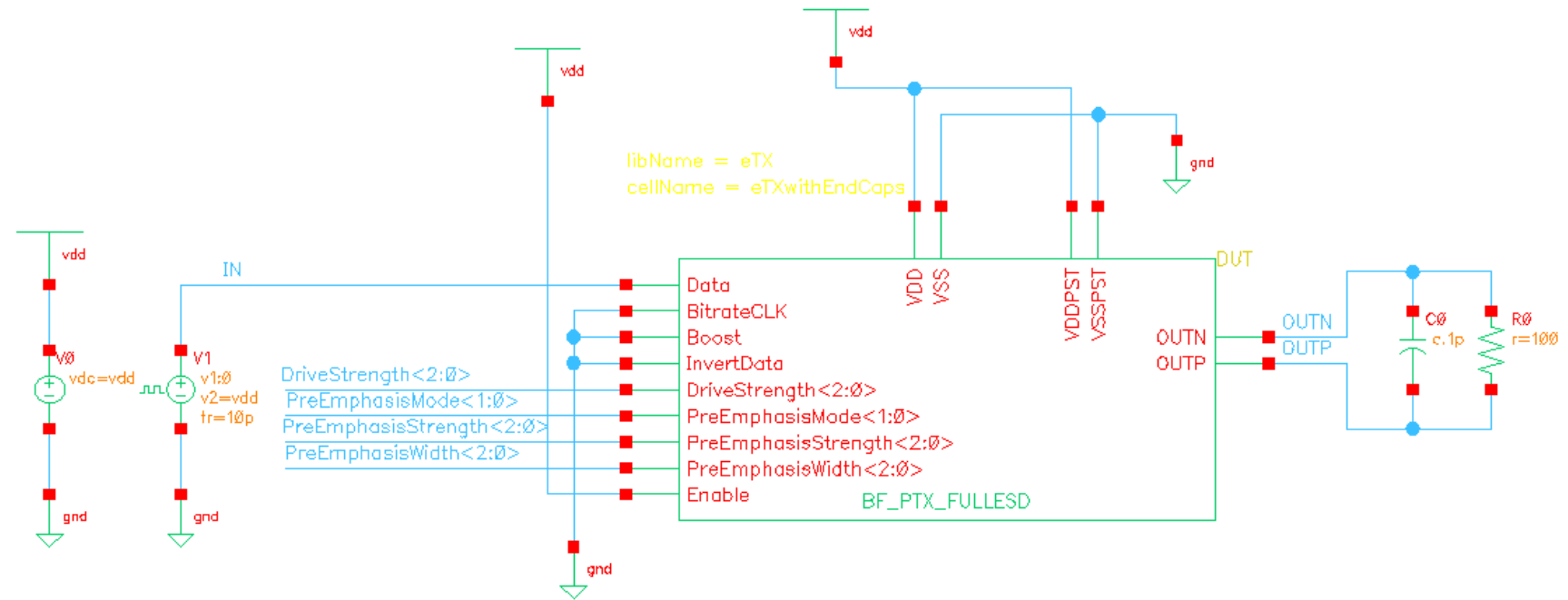
- VOLTUS-FI installed
- Files (check appendix):
 - Technology mapping file: pvtech.lib
 - PVS_QRC rules files for typical, best and worst cases
 - Electromigration models files for typical, best and worst cases
 - crn65lp_1p06m+alrdl_typical_em.ict
 - crn65lp_1p06m+alrdl_rcbest_em.ict
 - crn65lp_1p06m+alrdl_rcworst_em.ict
 - DFII layermap file: DFIIlayermap2.txt
 - Empty sub-circuit netlist files for devices without models
 - rnpolys_sub_circuit.spi, rnpolywo_m_sub_circuit.spi

Create Schematic and Symbol

VDD VSS OUTP
VDDPST VSSPST OUTN

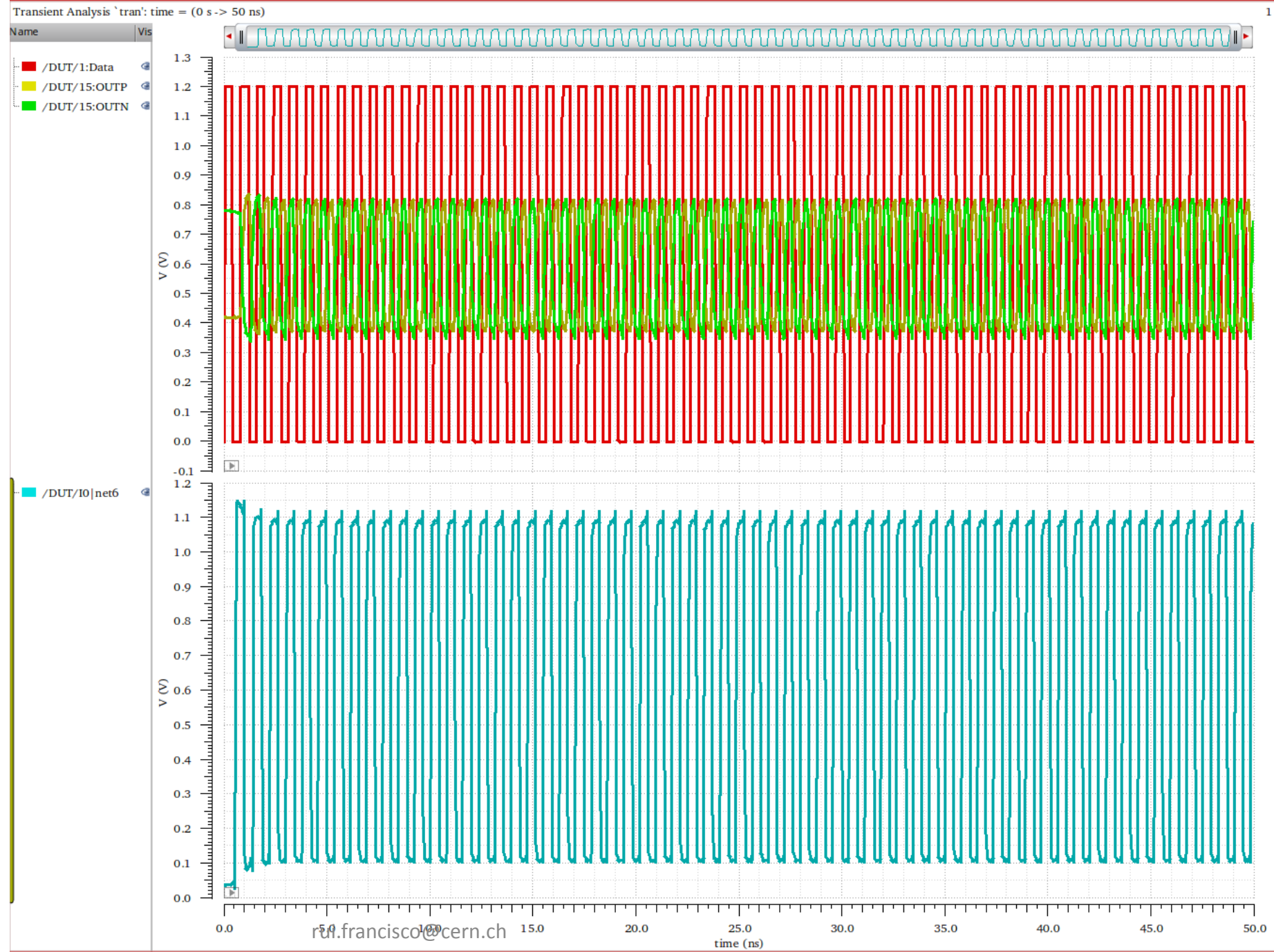


Create Test Bench

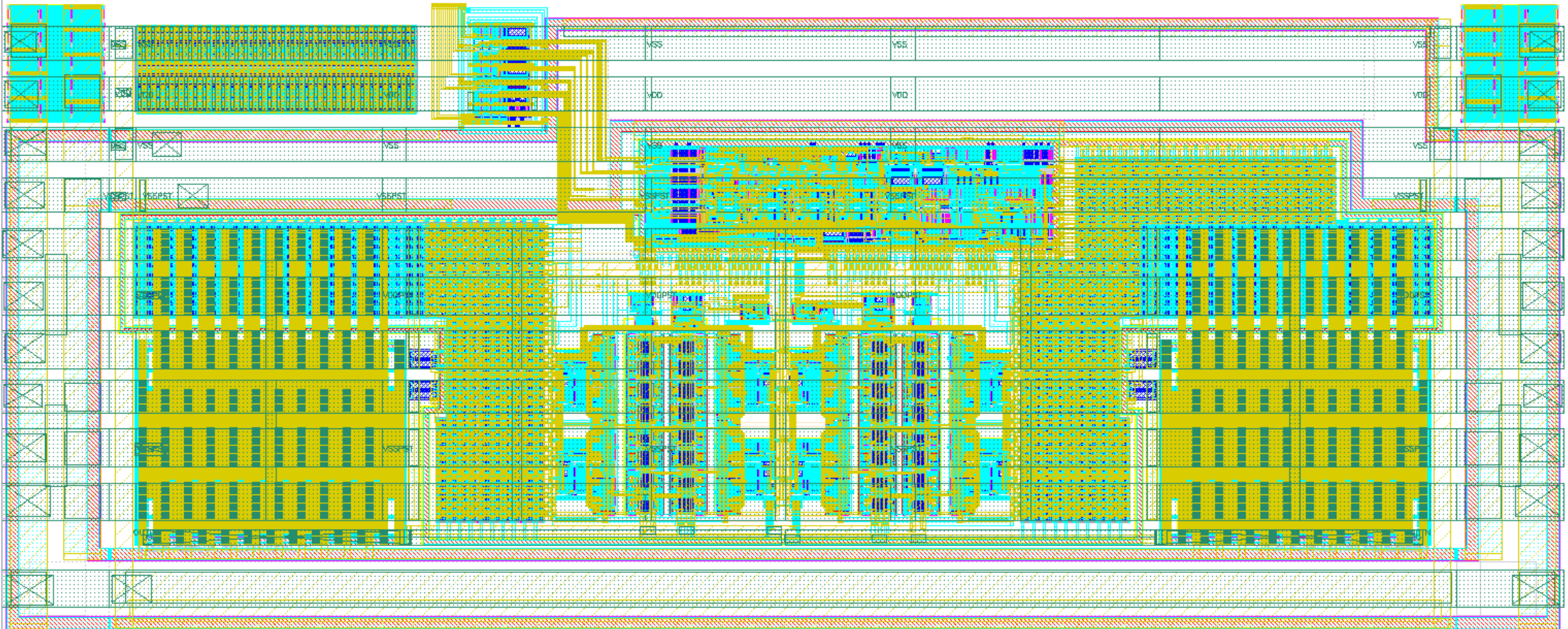


And Simulate

- Use ADEXL to setup schematic simulation

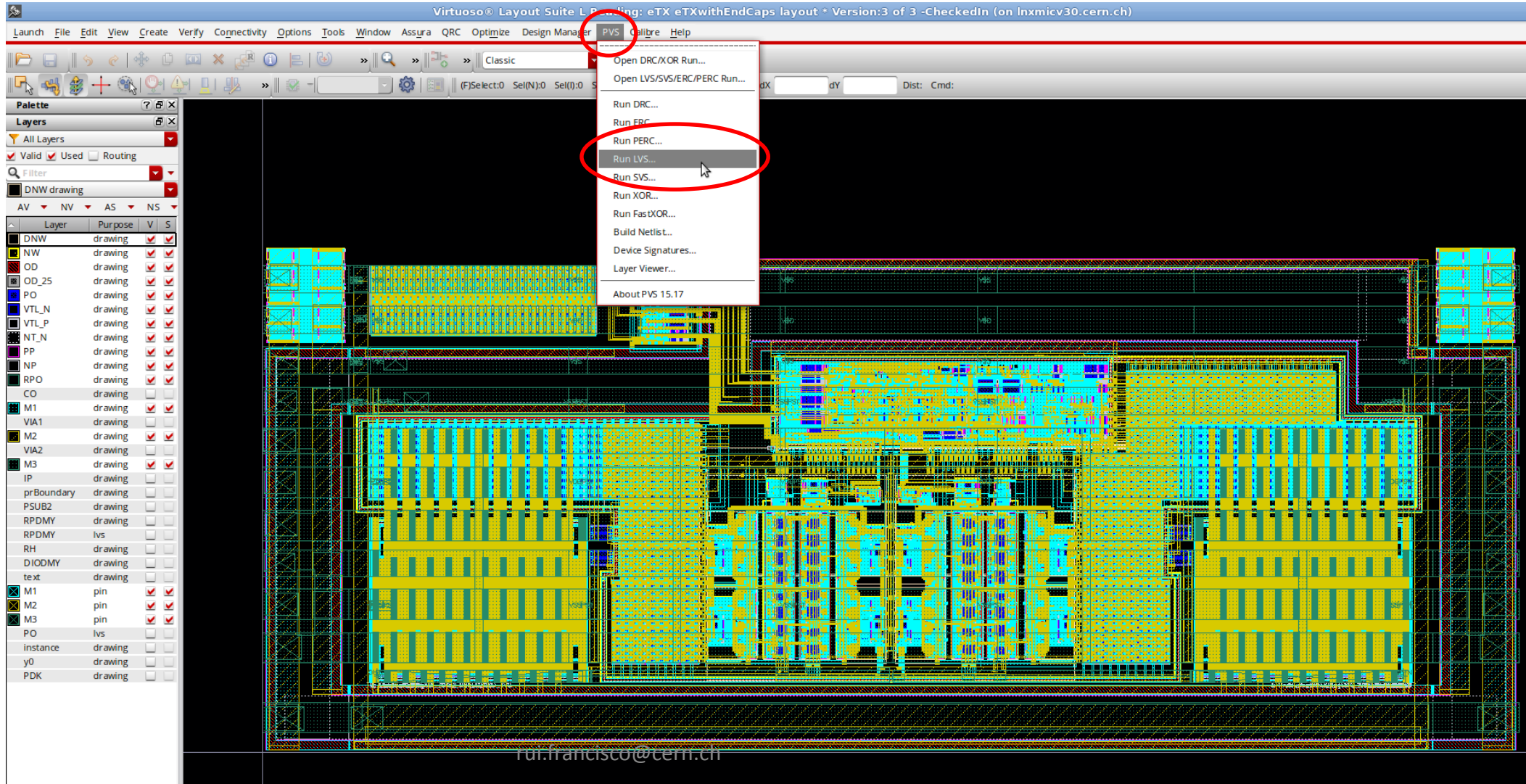


Create Layout



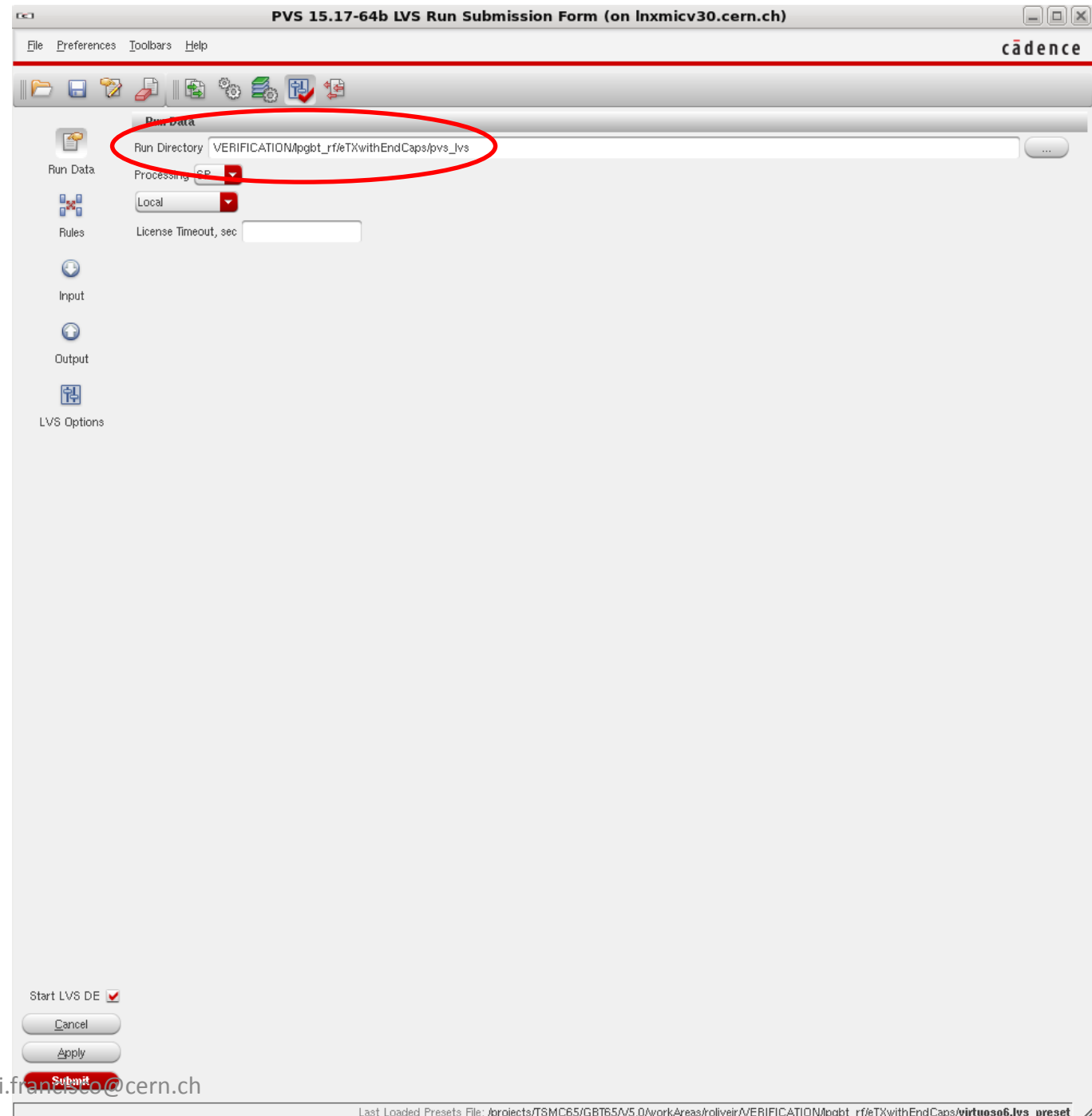
Run LVS using PVS

Virtuoso - Menu



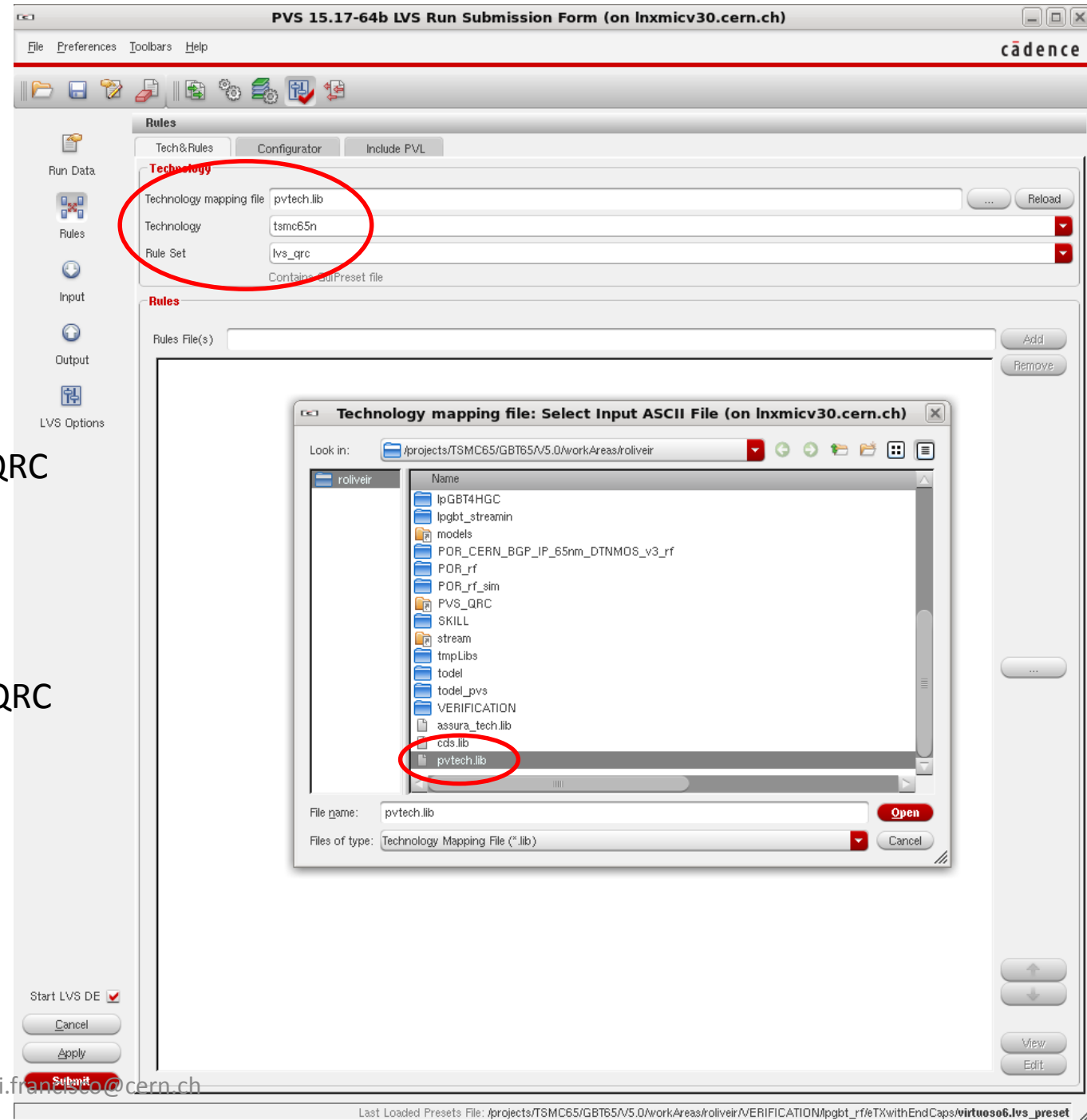
Run LVS using PVS Setup - Run Data

- Setup “Run Directory”



Run LVS using PVS Setup - Rules

- Find and select “pvtech.lib” file
- “pvtech.lib” file contains the path to the PVS_QRC technology/configuration files:
“DEFINE tsmc65n ./PVS_QRC”
- ./PVS_QRC is a link to:
(TSMC65 installation path)/1p6m3x1z1u/PVS_QRC
- Select Technology: tsmc65n
- Select Rule Set: lvs_qrc

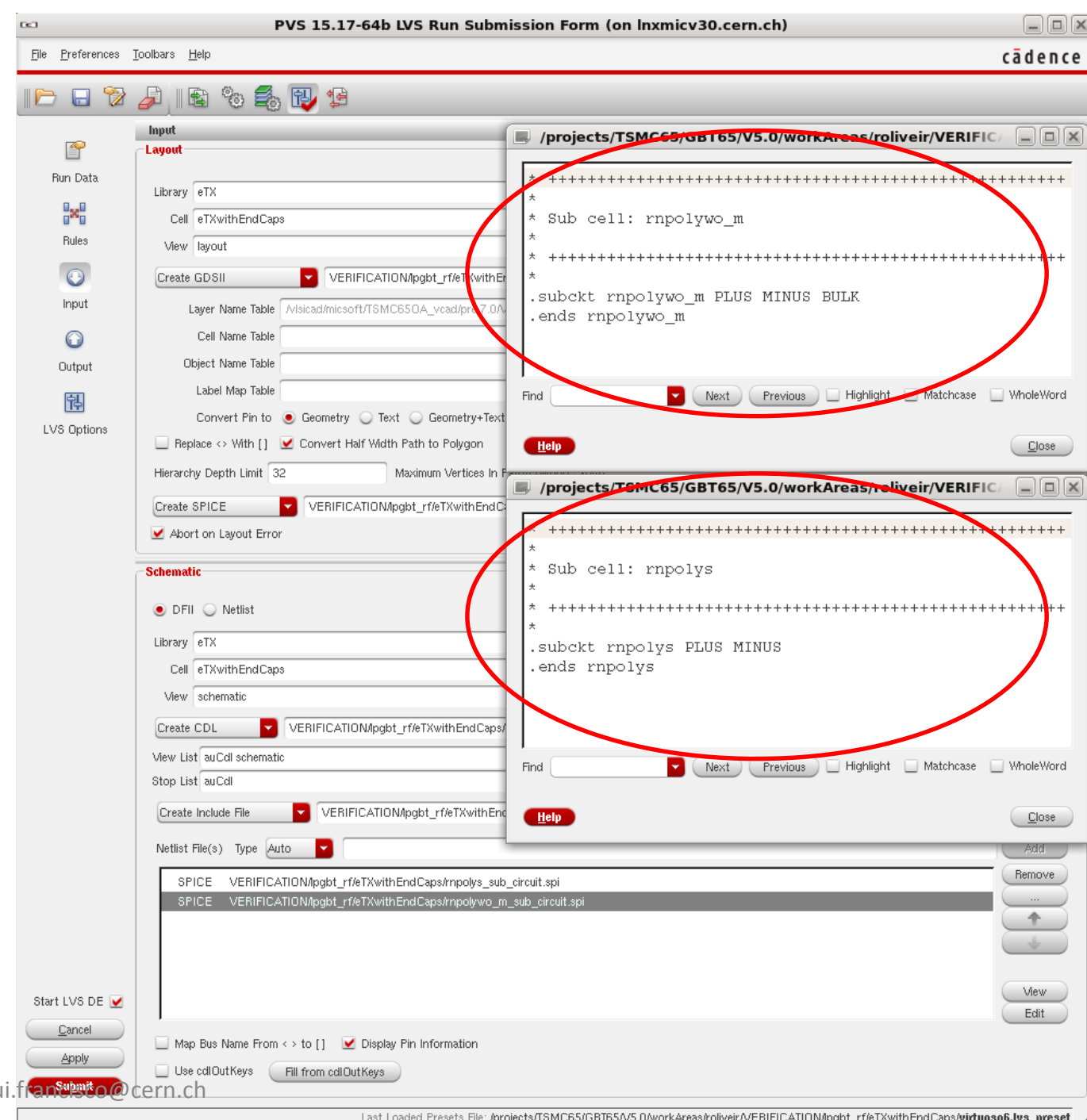


- Default options should work to create the GDSII file and the SPICE netlist from layout
- Default options should work to create CDL file
- If needed, include SPICE netlist files

Submit

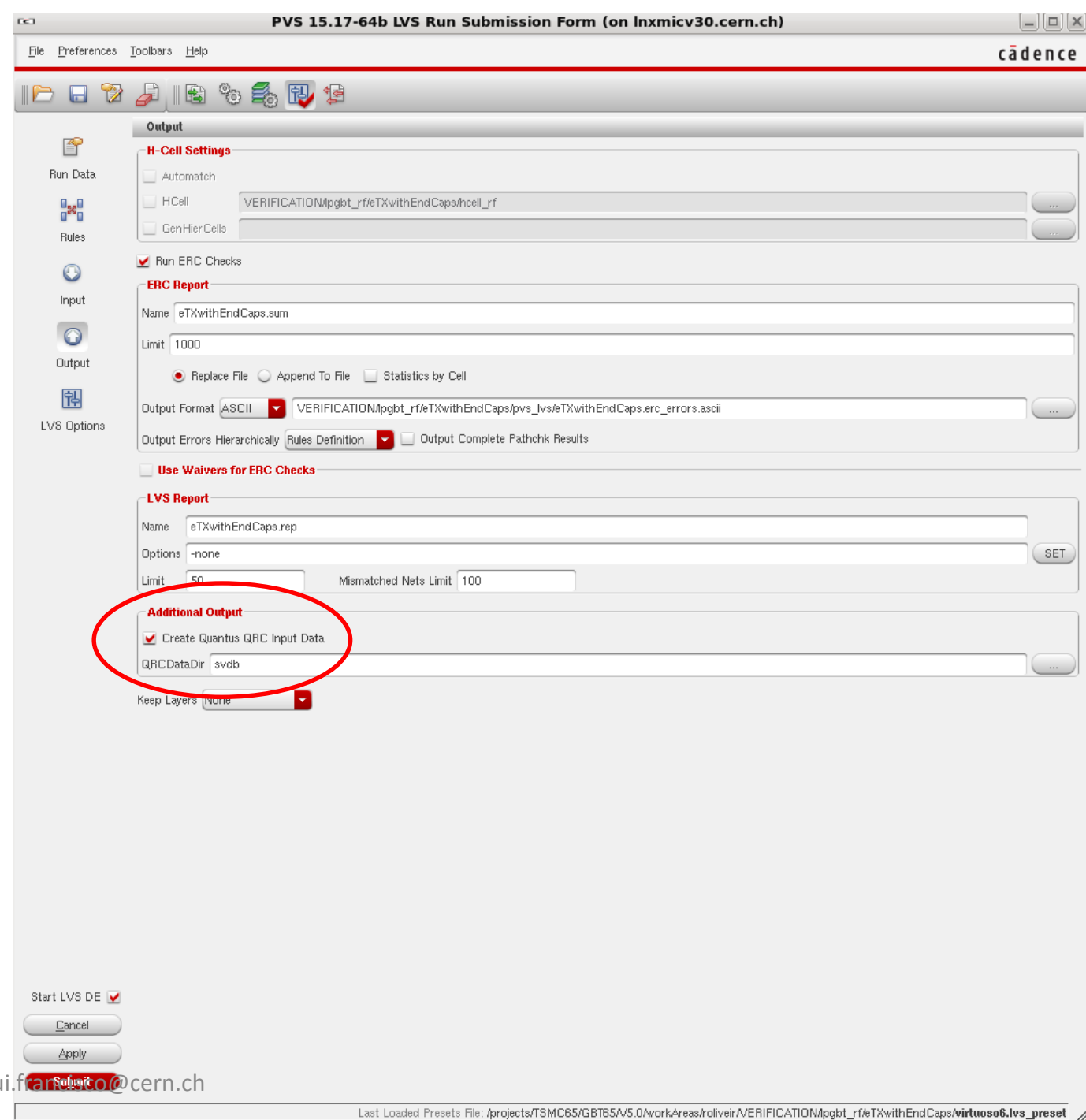
Run LVS using PVS Setup - SPICE files

- Empty sub-circuit netlist files can be added to filter non existing models



Run LVS using PVS Setup - Output

- Select “Create Quantus QRC Input Data”
- “svdb” folder will be created inside “Run Directory” already setup in the “Run Data” tab

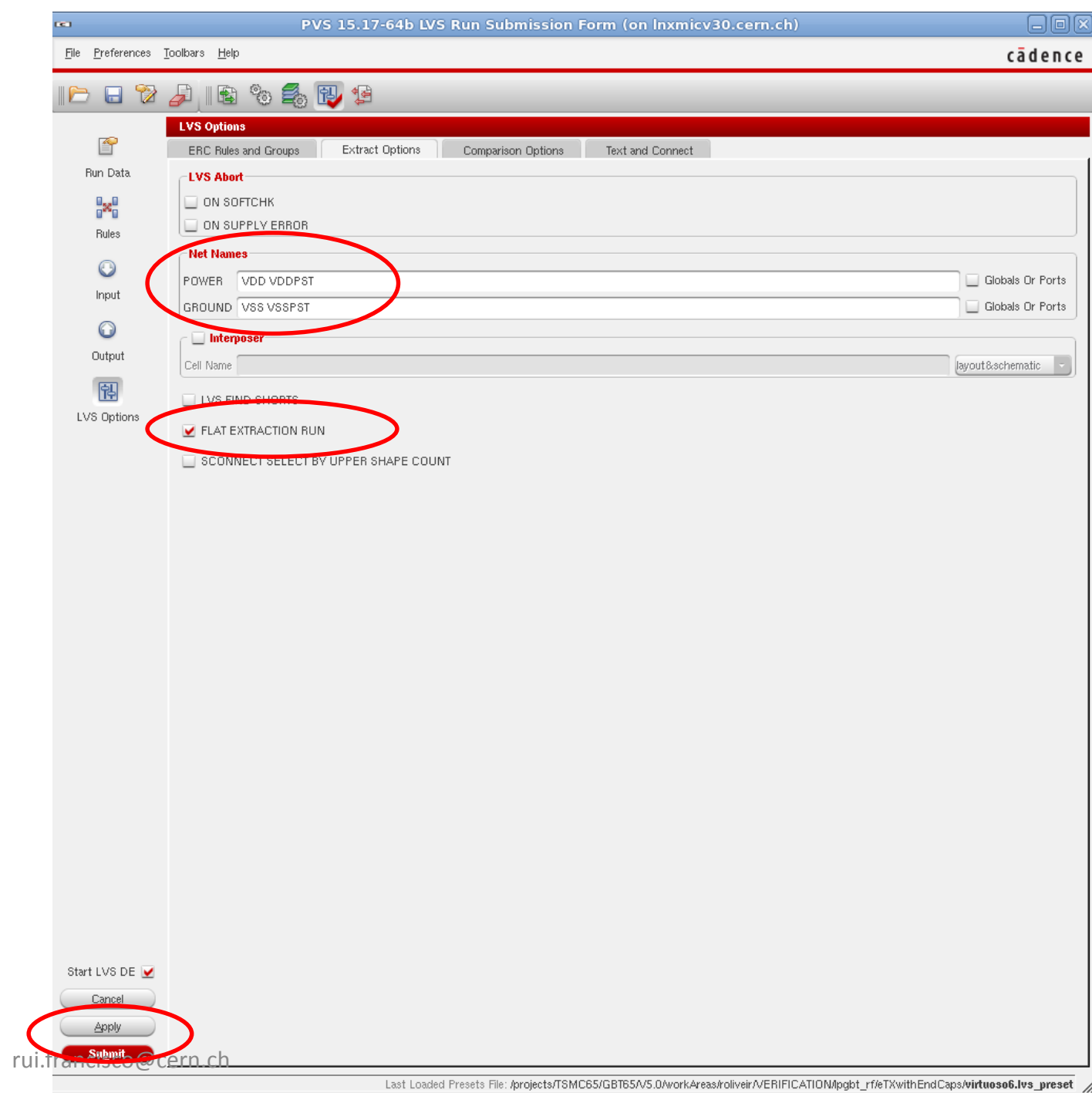


Run LVS using PVS Setup - LVS Options

- Add Power and Ground net names
- Select Flat Extraction Run

- Click Apply or Submit

20/05/2019



Run LVS using PVS

LVS Results

- LVS should MATCH

The screenshot shows the PVS 15.17-64b Reports: Done [LVS] pvs_lvs (on lnxmicv30.cern.ch) window. The main text area displays the LVS results, which are summarized in the following table:

Field	Value
Run Result	MATCH
Run Summary	[INFO] ERC Results: Empty [INFO] Extraction Clean
ERC Summary File	eTXwithEndCaps.sum
Extraction Report File	eTXwithEndCaps.rep
Comparison Report File	eTXwithEndCaps.rep.cls

Below the table, the text "PVS Comparison Finished. Mon May 20 15:46:48 2019" is displayed. The "Creating cross reference ..." section shows the following information:

```
pvs_RCXxref 15.17-s604 64 bit (Fri Jun 24 15:14:35 PDT 2016)
Build Ref No.: 604 Production (06-24-2016) [pvs_1517]
```

The "Copyright 2016 Cadence Design Systems, Inc. All rights reserved worldwide." section is also visible. The "Build O/S:" section shows the following information:

```
Build O/S: Linux x86_64 2.6.18-194.el5
Executed on: lnxmicv30.cern.ch (Linux x86_64 3.10.0-957.1.3.el7.x86_64)
Starting Time: Mon May 20 15:46:48 2019 (Mon May 20 13:46:48 2019 GMT)
With parameters: -format C /projects/TSMC65/GBT65/V5.0/workAreas/roliveir/VERIFICATION/lpgbt_rf/eTXw
```

The "Total CPU Time" section shows the following information:

```
Total CPU Time : 0(s)
Total Real Time : 0(s)
Memory Used : 59.11(M)
```

The "pvs_RCXxref Done" section shows the following information:

```
pvs_RCXxref Done
Checking in all SoftShare licenses.
```

The "Run Status" dialog box is open, showing a green checkmark and the following information:

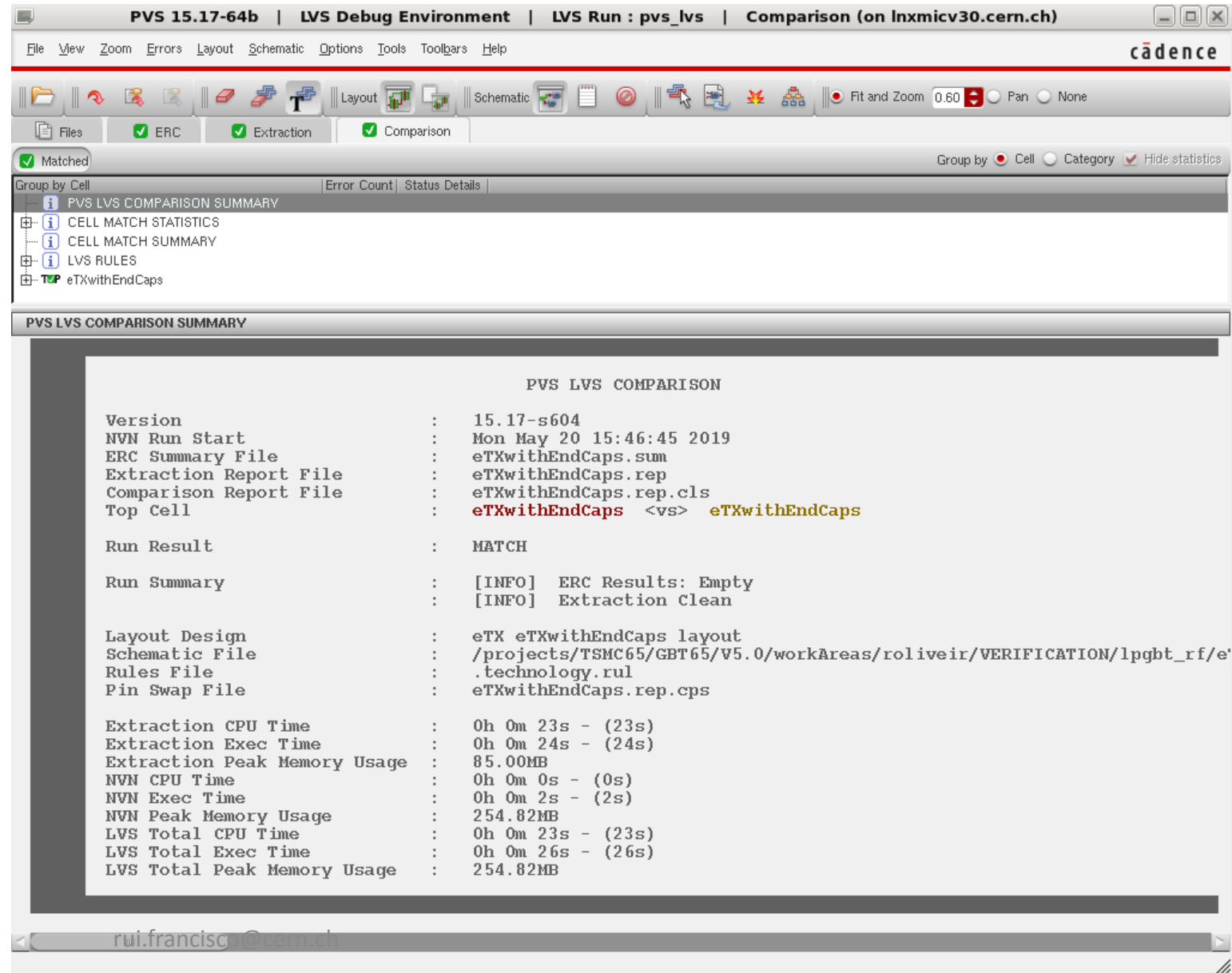
Field	Value
ERC Results	Empty
Extraction Results	Clean
Comparison Results	Match

The dialog box also includes a "Do you want to start the LVS DE?" question with "Yes" and "No" buttons. The "No" button is highlighted in red.

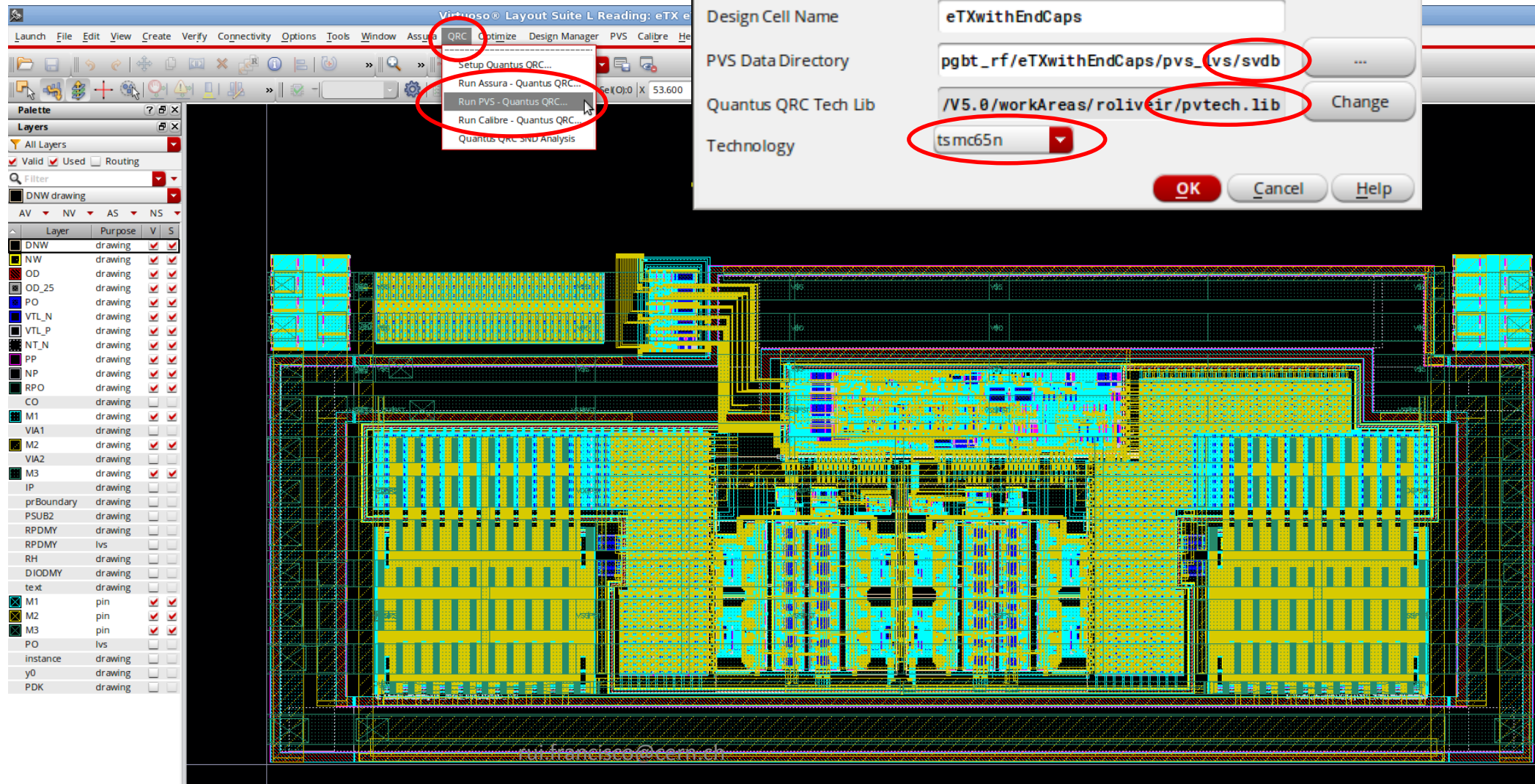
The bottom of the window shows a "Find" bar with a search icon, a "Next" button, a "Previous" button, and checkboxes for "Highlight", "Matchcase", and "Whole word". The "Error List" button is also visible. The status bar at the bottom shows the email address "rui.franco@cern.ch" and the file path "/projects/TSMC65/GBT65/V5.0/workAreas/roliveir/VERIFICATION/lpgbt_rf/eTXwithEndCaps/pvs_lvs".

Run LVS using PVS LVS DE

- If LVS doesn't MATCH, LVS Debug Environment should be used to correct existing issues

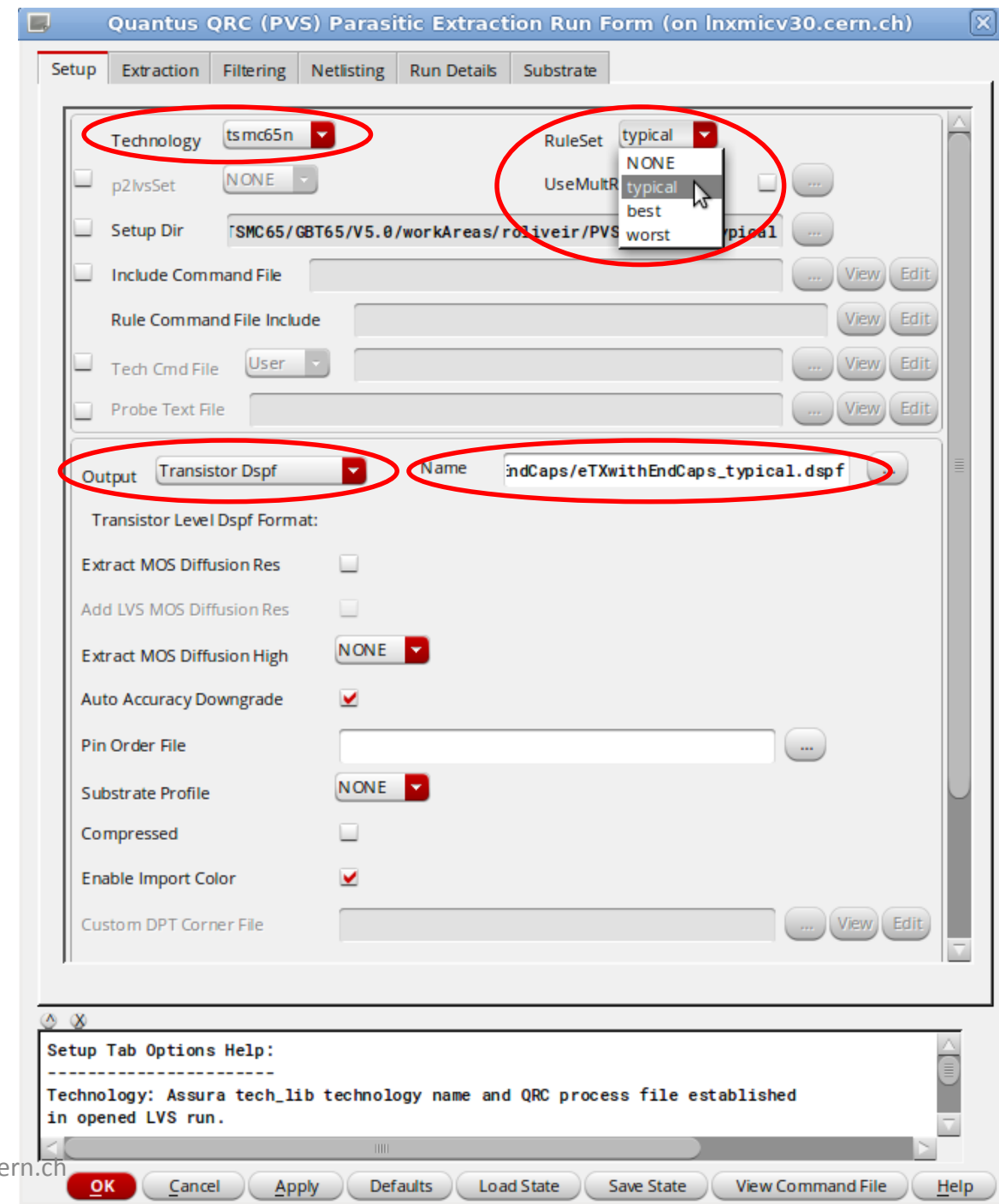


Run Quantus QRC using PVS - Menu



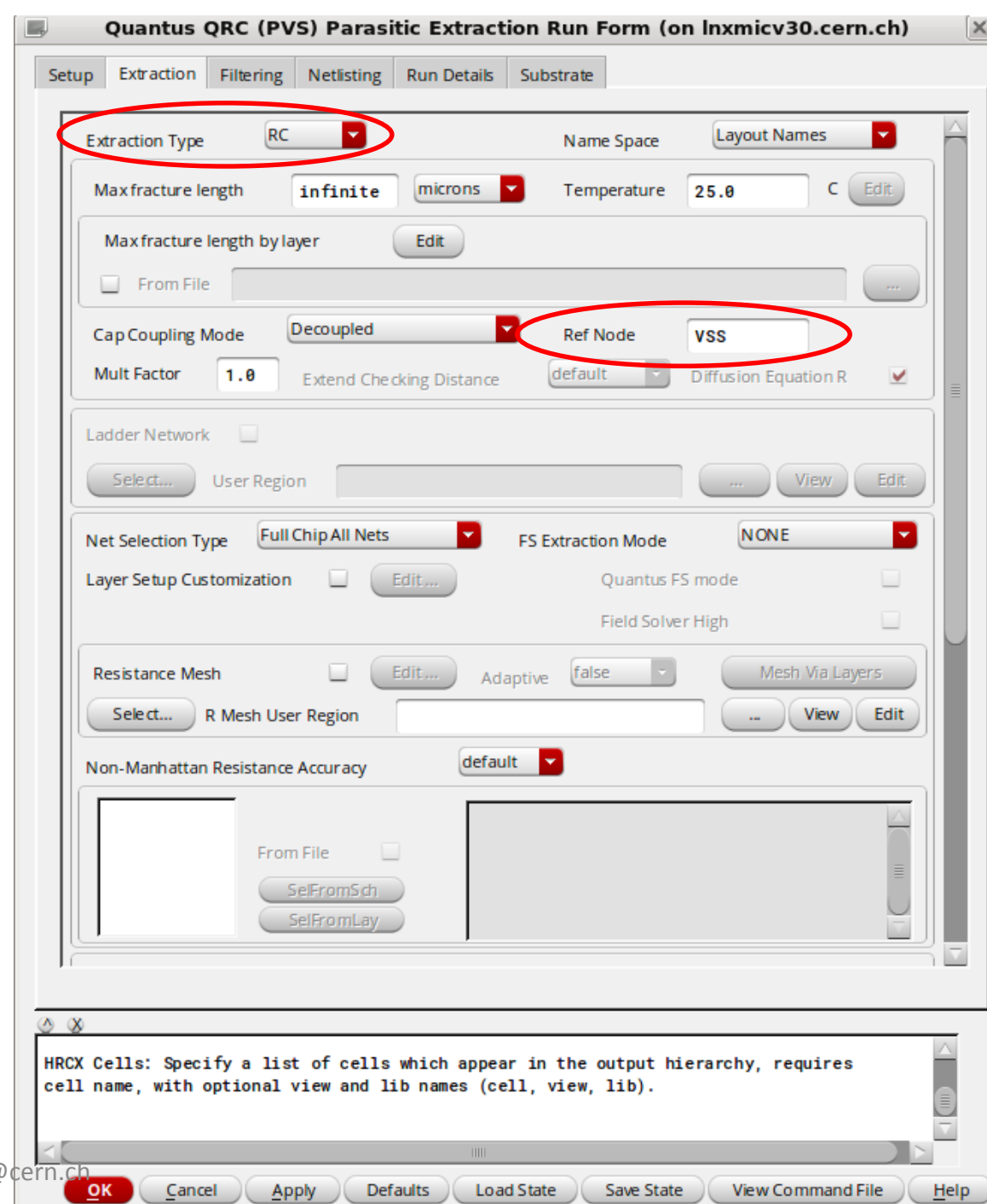
Run Quantus QRC using PVS - Setup

- Setup Technology and RuleSet
- Select “Transistor Dspf” for Output type
- Three runs can be executed to create “typical”, “best” and “worst” parasitic RC DSPF files



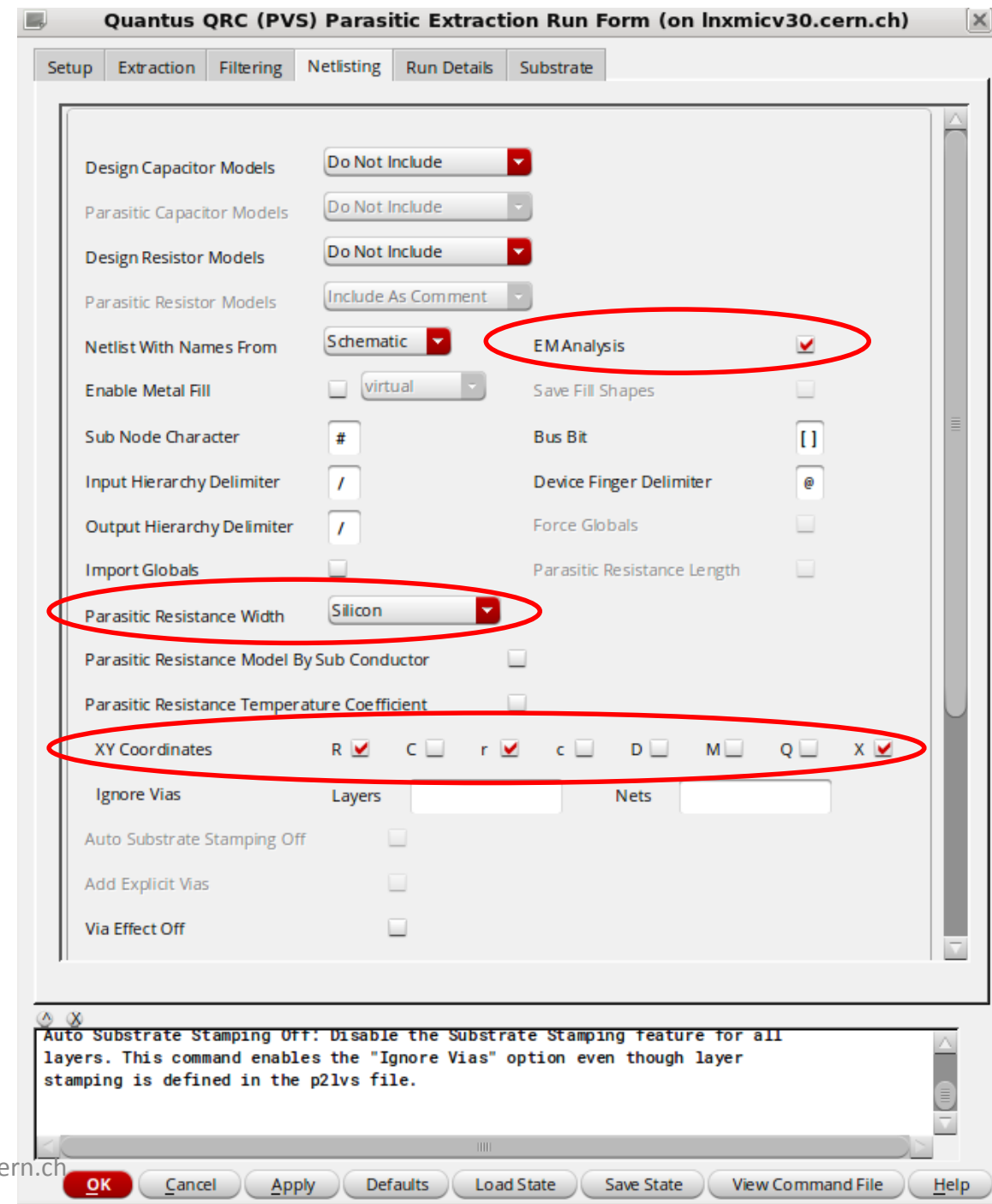
Run Quantus QRC using PVS - Extraction

- Select RC Extraction Type
- Add Reference Node



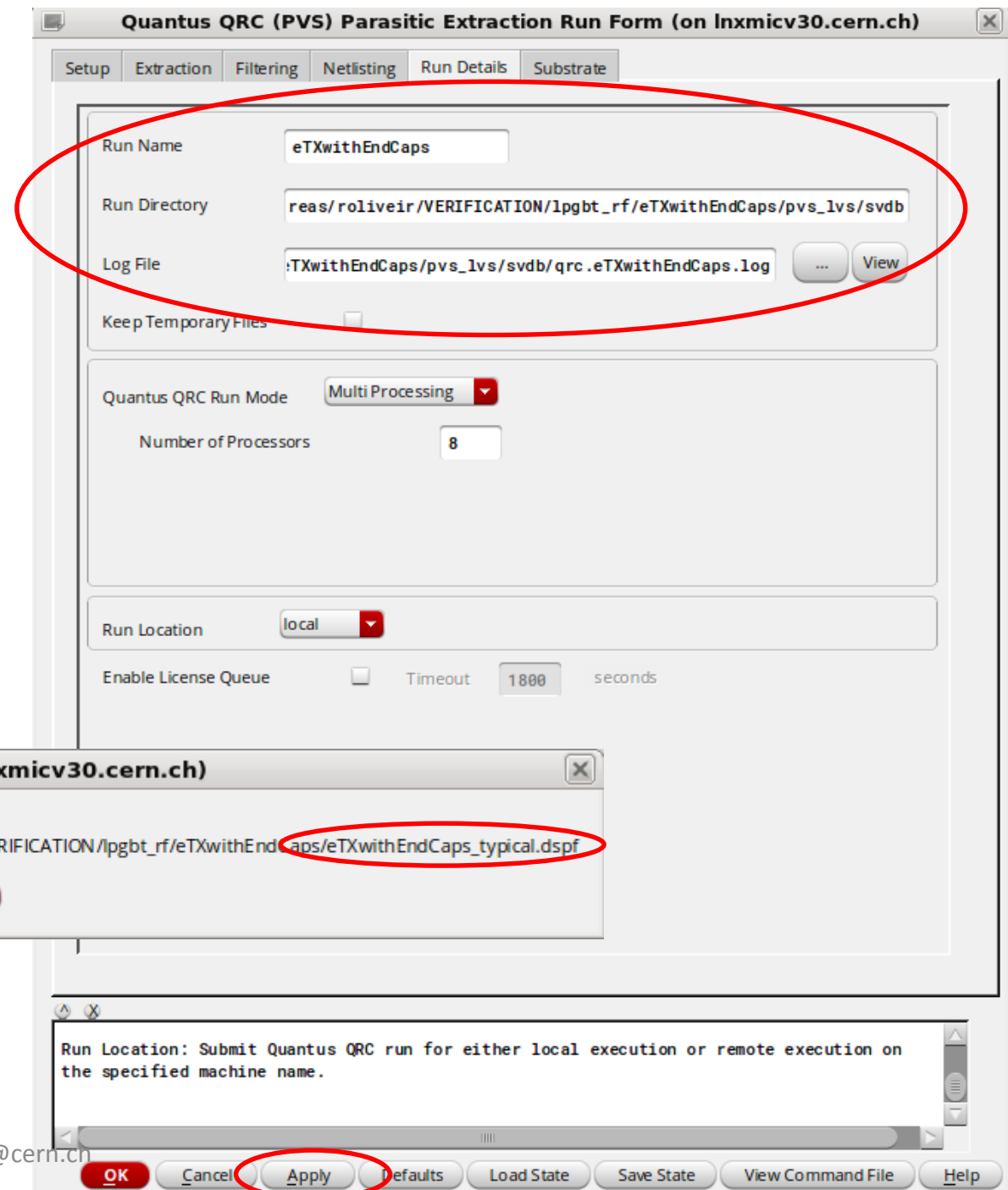
Run Quantus QRC using PVS - Netlisting

- Select “EM Analysis”
- Select “Silicon” for “Parasitic Resistance Width”
- Select XY Coordinates for the parasitics



Run Quantus QRC using PVS - Run Details

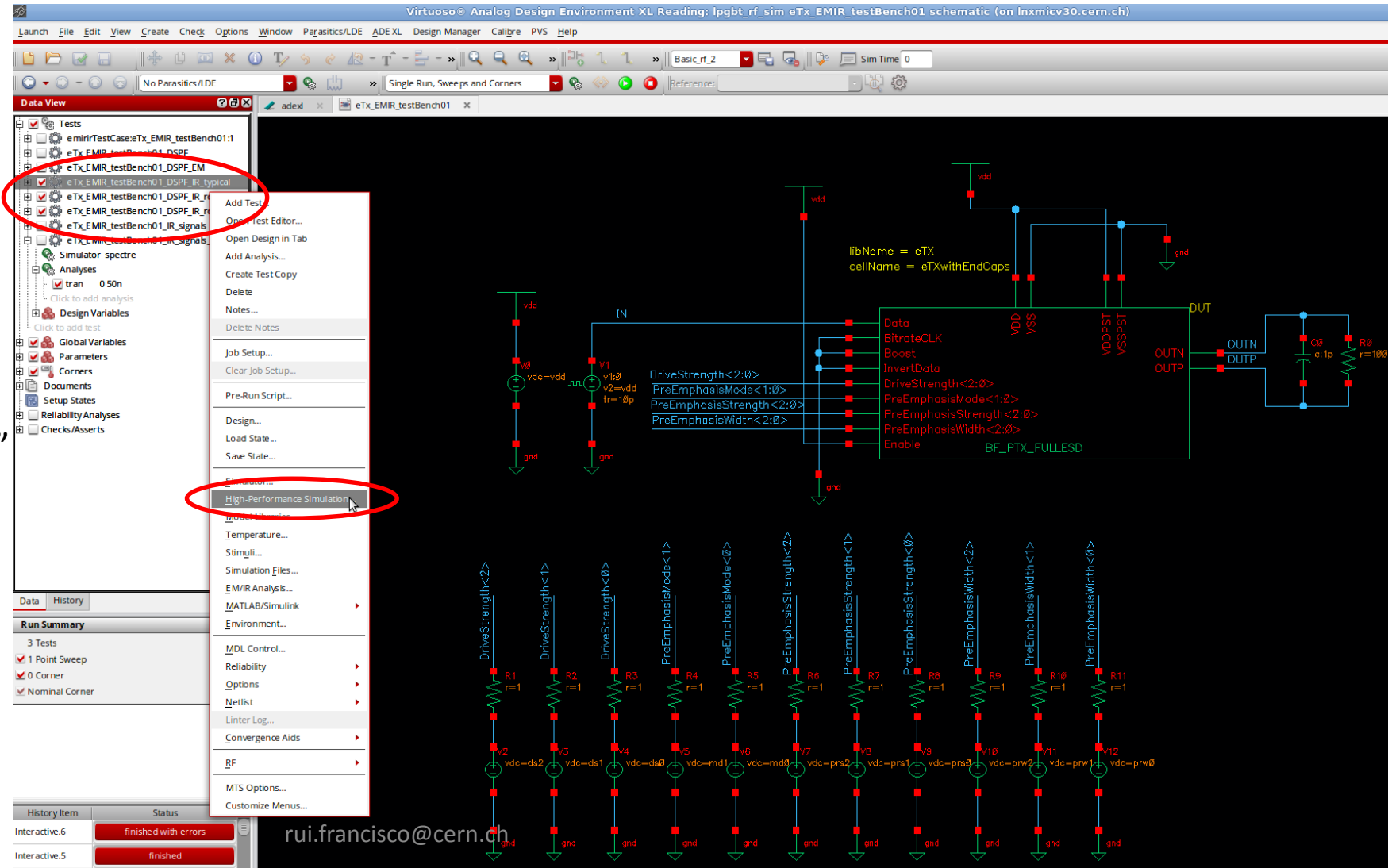
- Check “Run Details” and click Apply
- Quantus QRC Run should complete successfully



Run Simulation ADEXL

High Performance Simulation

- Open the previously used ADEXL view
- Select the previously used Test or create new ones
- Three test cases can be created for “typical”, “best” and “worst” DSPF files
- RMB test name and select “High-Performance Simulation”



Run Simulation ADEXL APS Options

- Select “APS”, “Do not override” and “Auto”

The screenshot shows a dialog box titled "High-Performance Simulation Options (on Inxmicv30.cern.ch)". It contains several sections with radio button and checkbox options. Red circles highlight the "APS" option under "Simulation Performance Mode", the "Do not override" option under "Error Preset", and the "Auto" option under "Multi-Threading".

Simulation Performance Mode
☐ Spectr ☒ APS ☐ XPS MS

General

Accuracy + Speed

Error Preset: ☒ Do not override ☐ Liberal ☐ Moderate ☐ Conservative

APS Options

Use ++aps: ☐

Multi-Threading

☒ Auto ☐ Disable ☐ Manual # Threads:

Processor affinity (e.g. 0-3 or 0,2,4,6):

Post-Layout Settings

Enable Post-Layout Optimization: ☐

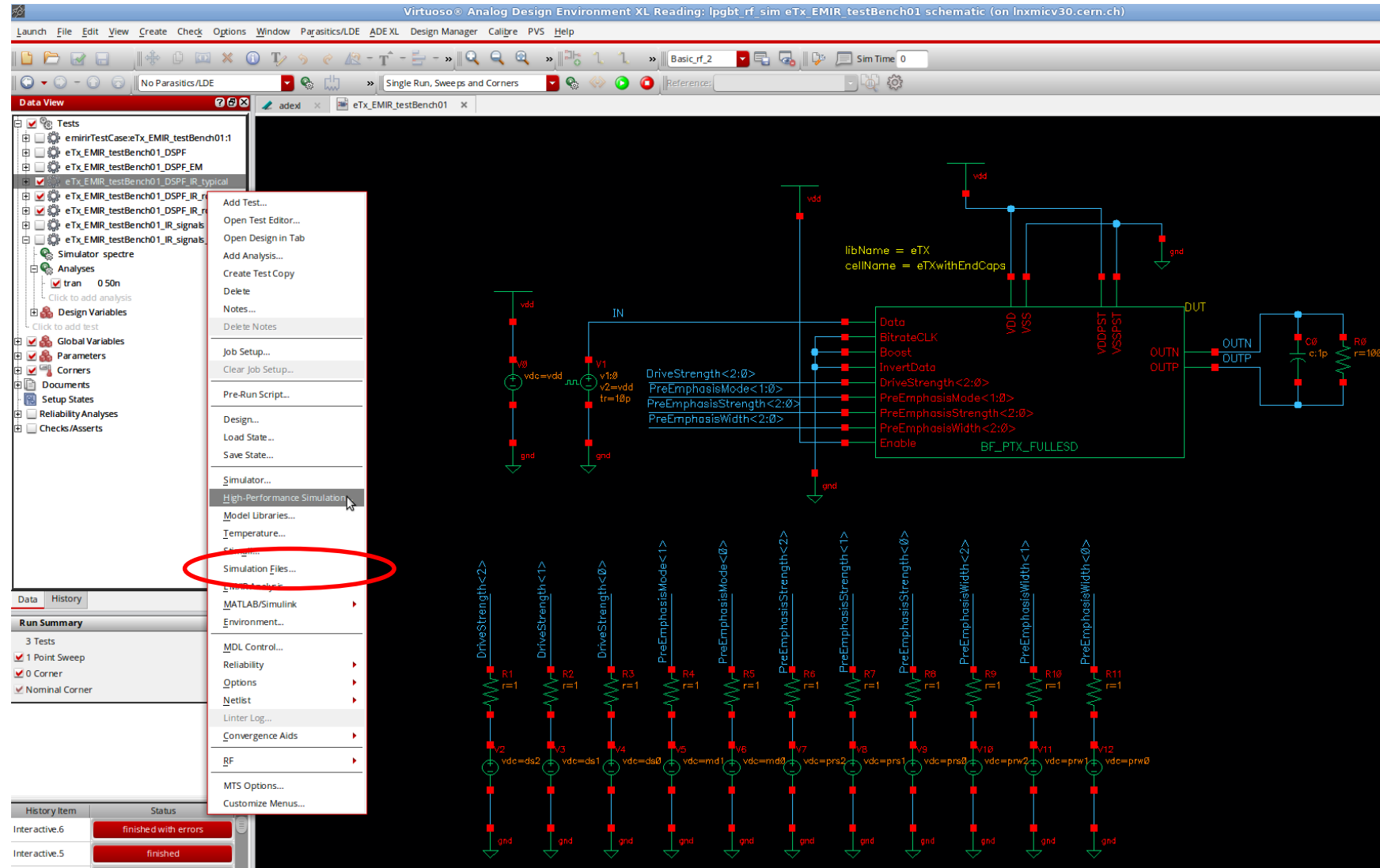
Post-Layout Preset Mode: ☒ Default ☐ High Precision Analog ☐ Ultra Precision Analog
☐ Legacy RCR ☐ Legacy-RF RCR

Instance Preservation: ☒ None ☐ Selected ☐ All

Selected Instances:

Run Simulation ADEXL Simulation Files - DSPF

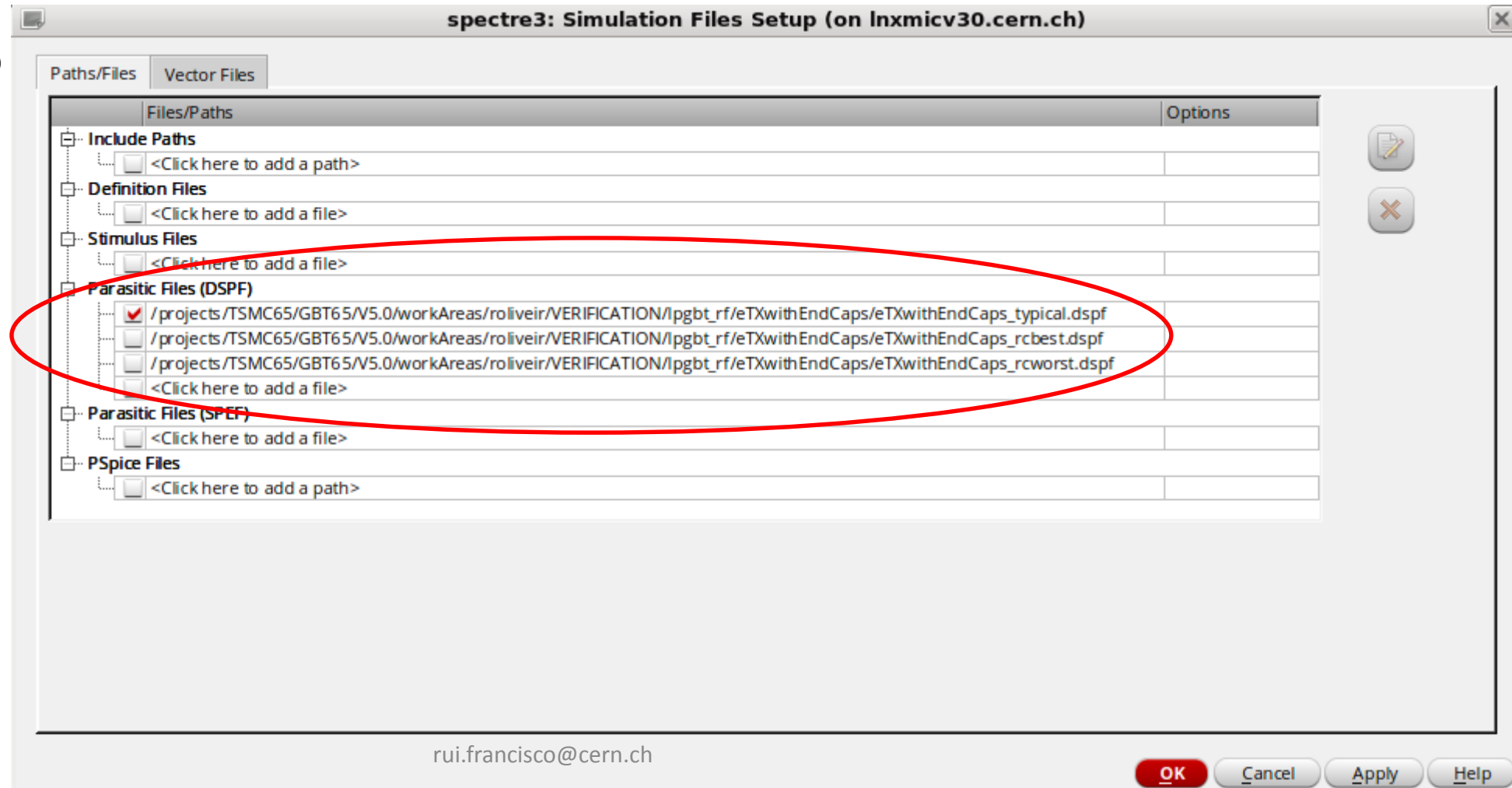
- RMB test name and select “Simulation Files”



Run Simulation ADEXL

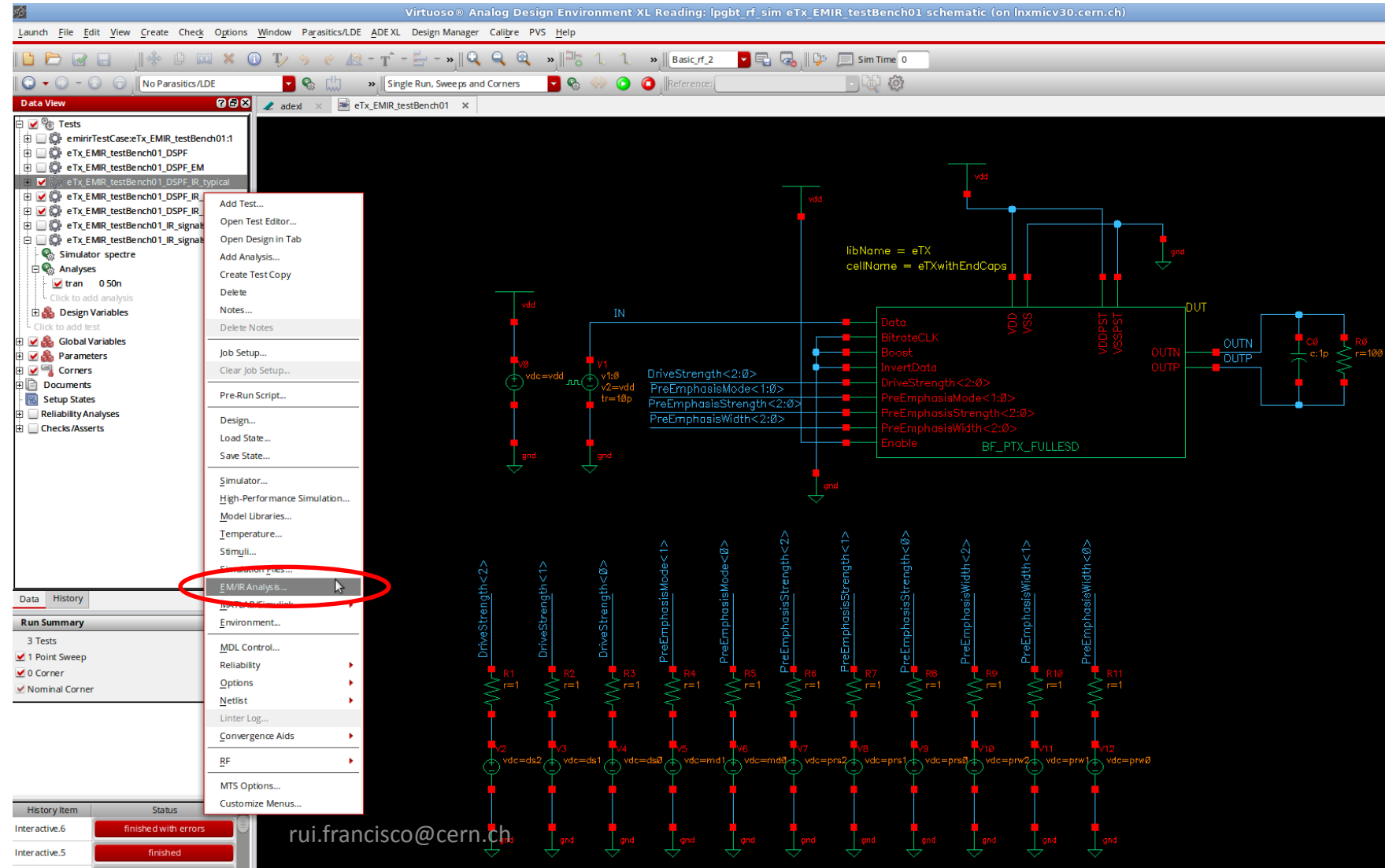
Simulation Files - DSPF

- Add DSPF files to “Parasitic Files”
- Select DSPF file according to test case



Run Simulation ADEXL EM/IR Analysis

- RMB test name and select “EM/IR Analysis”



Run Simulation ADEXL Setup - Analysis

- Select Type of Analysis
- Select Nets
- Select Type of Analysis for the Nets
- Default configuration allows:
 - IR Power Analysis
 - EM Power and Signals Analysis
- Browse for and Select the adequate “*_em.ict” file
- Select “Enable EMIR Analysis in Transient or DC Simulation”

spectre3: EM/IR Analysis Setup (on Inxmicv30.cern.ch)

Analysis Solver Options Macro Model Generation

Type ☒ Dynamic ☐ Static

Net Selection

Net Name: DUT.VSS DUT.VSSPST DUT.VDD DUT.VDDPST or DUT.* Select Clear

IR Drop Analysis: ☒ max ☒ avg EM Current Analysis: ☒ max ☐ avg ☒ avgabs ☒ rms

Advanced IR Drop Analysis: ☐ Signal Net IR Drop ☐ Power Gate

Analysis: ☐ TMI Selfheating Add/Modify

Emirutil Setup

EM Tech File eas/roliveir/VERIFICATION/crm65lp_1p06m+alrd1_typical_em.ict

Layer Map File

EM Only ICT File

Summary Information

Options	Value
emirutil	techfile=/projects/TSMC65/GBT65/V5.0/workAreas/roliveir/VERIFICATION/crm65lp_1p06m+alrd1_typical_em.ict
net	name=[DUT.VSS DUT.VSSPST DUT.VDD DUT.VDDPST] analysis=[vmax vavg imax iavg]
net	name=[DUT.*] analysis=[imax iavg iavgabs irms]
solver	method=[direct]
spf	alias term = "dnwpsub 1=POS 2=NEG"
spf	alias term = "nch 1=d 2=g 3=s"
spf	alias term = "nch_25 1=d 2=g 3=s"
spf	alias term = "nch_lvt 1=d 2=g 3=s"
spf	alias term = "ndio 1=POS 2=NEG"
spf	alias term = "nwdio 1=POS 2=NEG"
spf	alias term = "pch 1=d 2=g 3=s"

☒ Enable EMIR Analysis in Transient or DC Simulation

OK Cancel Apply Help

Run Simulation ADEXL Setup - Analysis

- Click Add/Modify if changes were done

spectre3: EM/IR Analysis Setup (on Inxmicv30.cern.ch)

Analysis Solver Options Macro Model Generation

Type ☒ Dynamic ☐ Static

Net Selection

Net Name:

IR Drop Analysis: ☒ max ☒ avg EM Current Analysis: ☒ max ☒ avg ☒ avgabs ☒ rms

Advanced IR Drop Analysis: ☐ Signal Net IR Drop ☐ Power Gate

Analysis: ☐ TMI Selfheating

Add net(s) to summary information

Emirutil Setup

EM Tech File

Layer Map File

EM Only ICT File

Summary Information

Options	Value
emirutil	techfile=/projects/TSMC65/GBT65/V5.0/workAreas/roliveir/VERIFICATION/crn651p_1p06m+alrd1_typical_em.ict
net	name=[DUT.VSS DUT.VSSPST DUT.VDD DUT.VDDPST] analysis=[vmax avgv imax iavg]
net	name=[DUT.*] analysis=[vmax avgv imax iavg iavgabs irms]
solver	method=[direct]
spf	aliasterm = "dnwpsub 1=POS 2=NEG"
spf	aliasterm = "nch 1=d 2=g 3=s"
spf	aliasterm = "nch_25 1=d 2=g 3=s"
spf	aliasterm = "nch_lvt 1=d 2=g 3=s"
spf	aliasterm = "ndio 1=POS 2=NEG"
spf	aliasterm = "nwdio 1=POS 2=NEG"
spf	aliasterm = "pch 1=d 2=g 3=s"

☒ Enable EMIR Analysis in Transient or DC Simulation

Run Simulation ADEXL Setup - Analysis

- For IR Signals Analysis select Advanced IR Drop Analysis: Signal Net IR Drop

spectre3: EM/IR Analysis Setup (on Inxmicv30.cern.ch)

Analysis Solver Options Macro Model Generation

Type ☒ Dynamic ☐ Static

Net Selection

Net Name: DUT.VSS DUT.VSSPST DUT.VDD DUT.VDDPST or DUT.* Select Clear

Analysis: ☒ sigvmax ☒ sigvavg Reference Type: ☒ max ☐ avg findsrc: ☐

Advanced IR Drop Analysis: ☒ Signal Net IR Drop ☐ Power Gate

Analysis: ☐ TMI Selfheating Add/Modify

Emirutil Setup

EM Tech File eas/roliveir/VERIFICATION/crn65lp_1p06m+alrd1_typical1_em.ict ...

Layer Map File ...

EM Only ICT File ...

Summary Information

Options	Value
emirutil	techfile=/projects/TSMC65/GBT65/V5.0/workAreas/roliveir/VERIFICATION/crn65lp_1p06m+alrd1_typical1_em.ict
net	name=[DUT.VSS DUT.VSSPST DUT.VDD DUT.VDDPST] analysis=[vmax vavg imax iavg]
net	name=[DUT.*] analysis=[imax iavg iavgabs irms]
solver	method=[direct]
spf	aliasterm = "dnwpsub 1=POS 2=NEG"
spf	aliasterm = "nch 1=d 2=g 3=s"
spf	aliasterm = "nch_25 1=d 2=g 3=s"
spf	aliasterm = "nch_lvt 1=d 2=g 3=s"
spf	aliasterm = "ndio 1=POS 2=NEG"
spf	aliasterm = "nwdio 1=POS 2=NEG"
spf	aliasterm = "pch 1=d 2=g 3=s"

☒ Enable EMIR Analysis in Transient or DC Simulation

Import Export Delete Clear

OK Cancel Apply Help

Run Simulation ADEXL Setup - Analysis

- Click Add/Modify if changes were done

spectre3: EM/IR Analysis Setup (on Inxmicv30.cern.ch)

Analysis Solver Options Macro Model Generation

Type ☒ Dynamic ☐ Static

Net Selection

Net Name:

IR Drop Analysis: ☒ max ☒ avg EM Current Analysis: ☒ max ☒ avg ☒ avgabs ☒ rms

Advanced IR Drop Analysis: ☐ Signal Net IR Drop ☐ Power Gate

Analysis: ☐ TMI Selfheating

Add net(s) to summary information

Emirutil Setup

EM Tech File

Layer Map File

EM Only ICT File

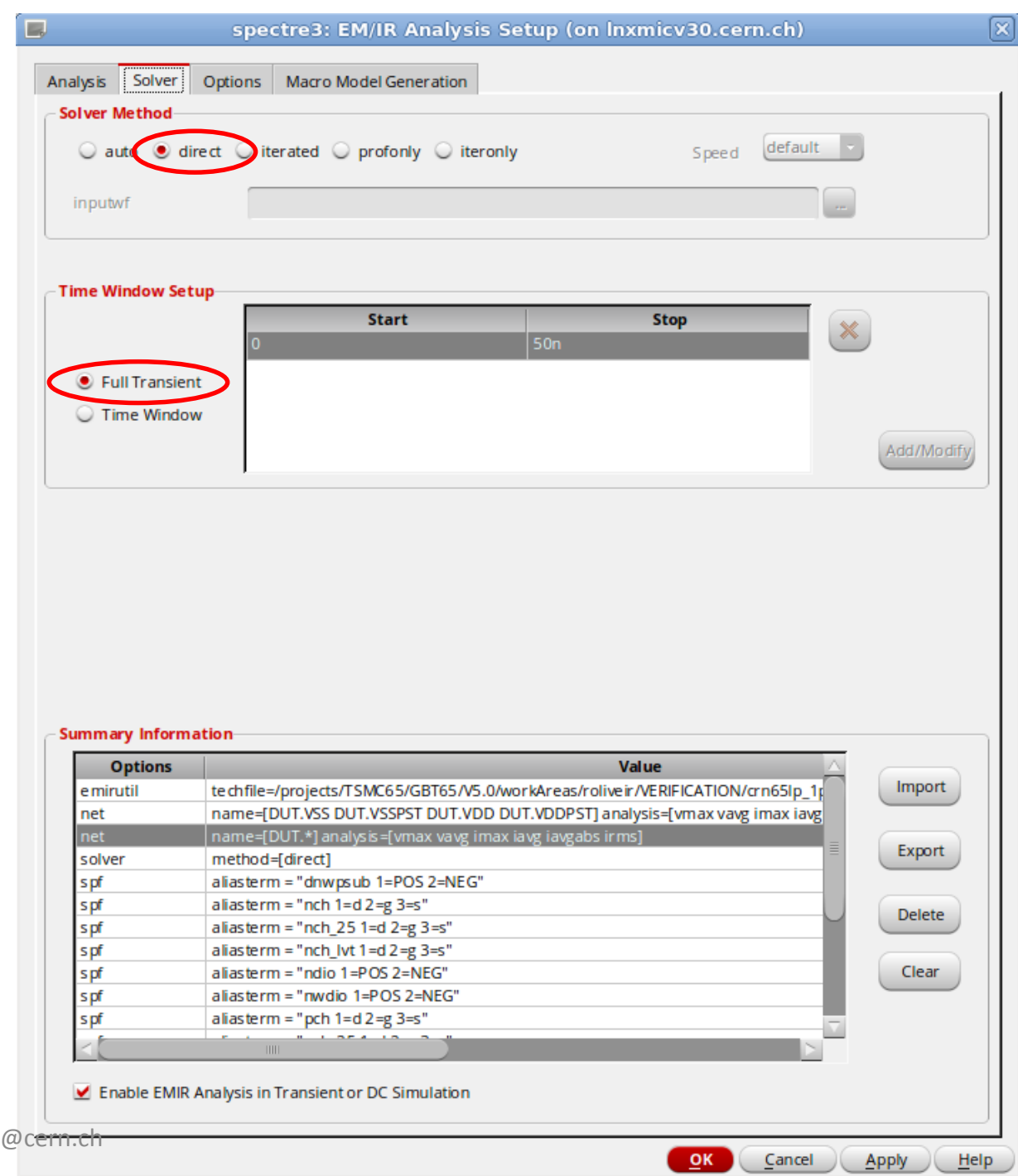
Summary Information

Options	Value
emirutil	techfile=/projects/TSMC65/GBT65/V5.0/workAreas/roliveir/VERIFICATION/crn651p_1p06m+alrd1_typical_em.ict
net	name=[DUT.VSS DUT.VSSPST DUT.VDD DUT.VDDPST] analysis=[vmax avgv imax iavg]
net	name=[DUT.*] analysis=[vmax avgv imax iavg iavgabs irms]
solver	method=[direct]
spf	aliasterm = "dnwpsub 1=POS 2=NEG"
spf	aliasterm = "nch 1=d 2=g 3=s"
spf	aliasterm = "nch_25 1=d 2=g 3=s"
spf	aliasterm = "nch_lvt 1=d 2=g 3=s"
spf	aliasterm = "ndio 1=POS 2=NEG"
spf	aliasterm = "nwdio 1=POS 2=NEG"
spf	aliasterm = "pch 1=d 2=g 3=s"

☒ Enable EMIR Analysis in Transient or DC Simulation

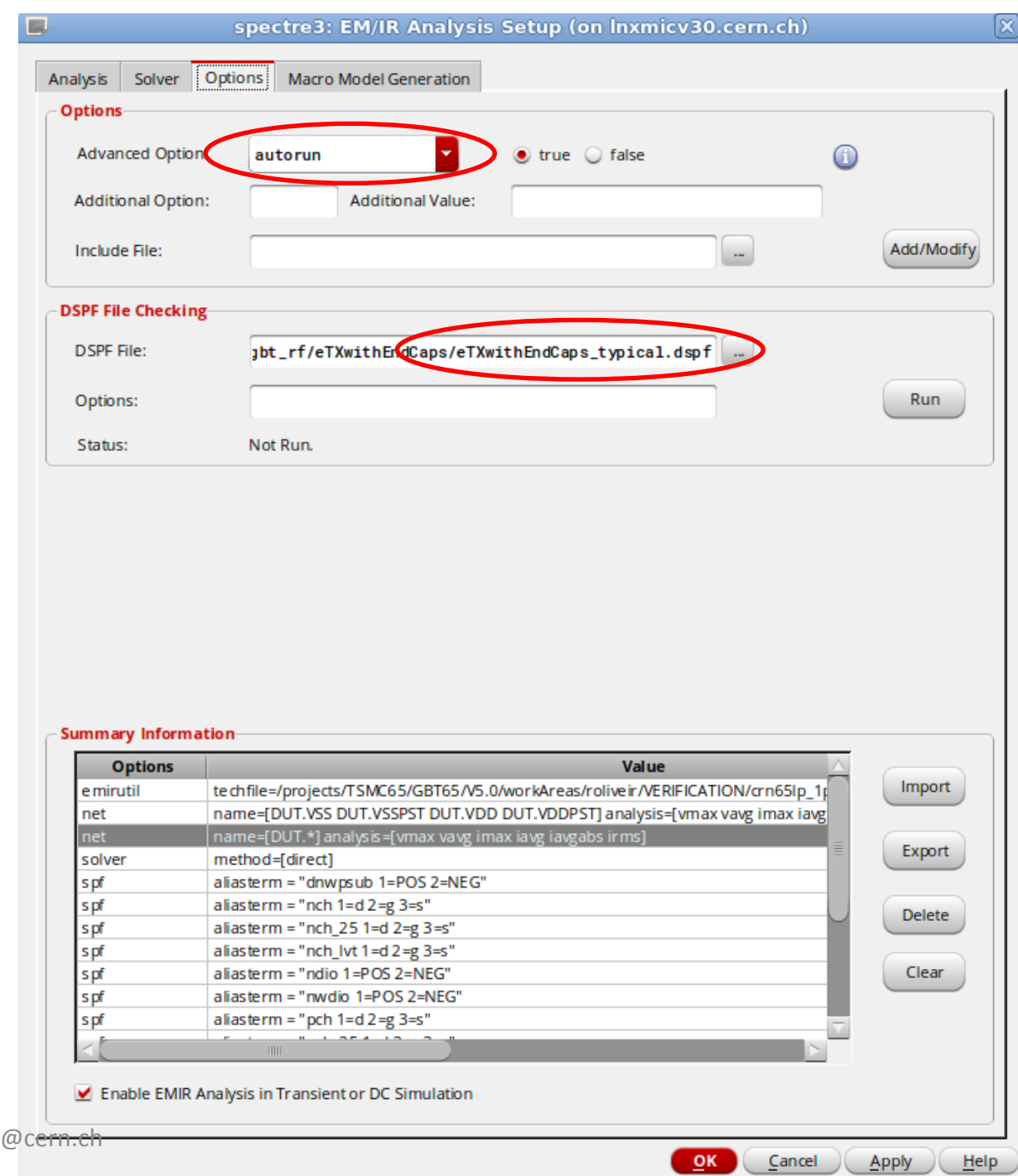
Run Simulation ADEXL Setup - Solver

- Select “direct” for Solver Method
- Choose the Time Window



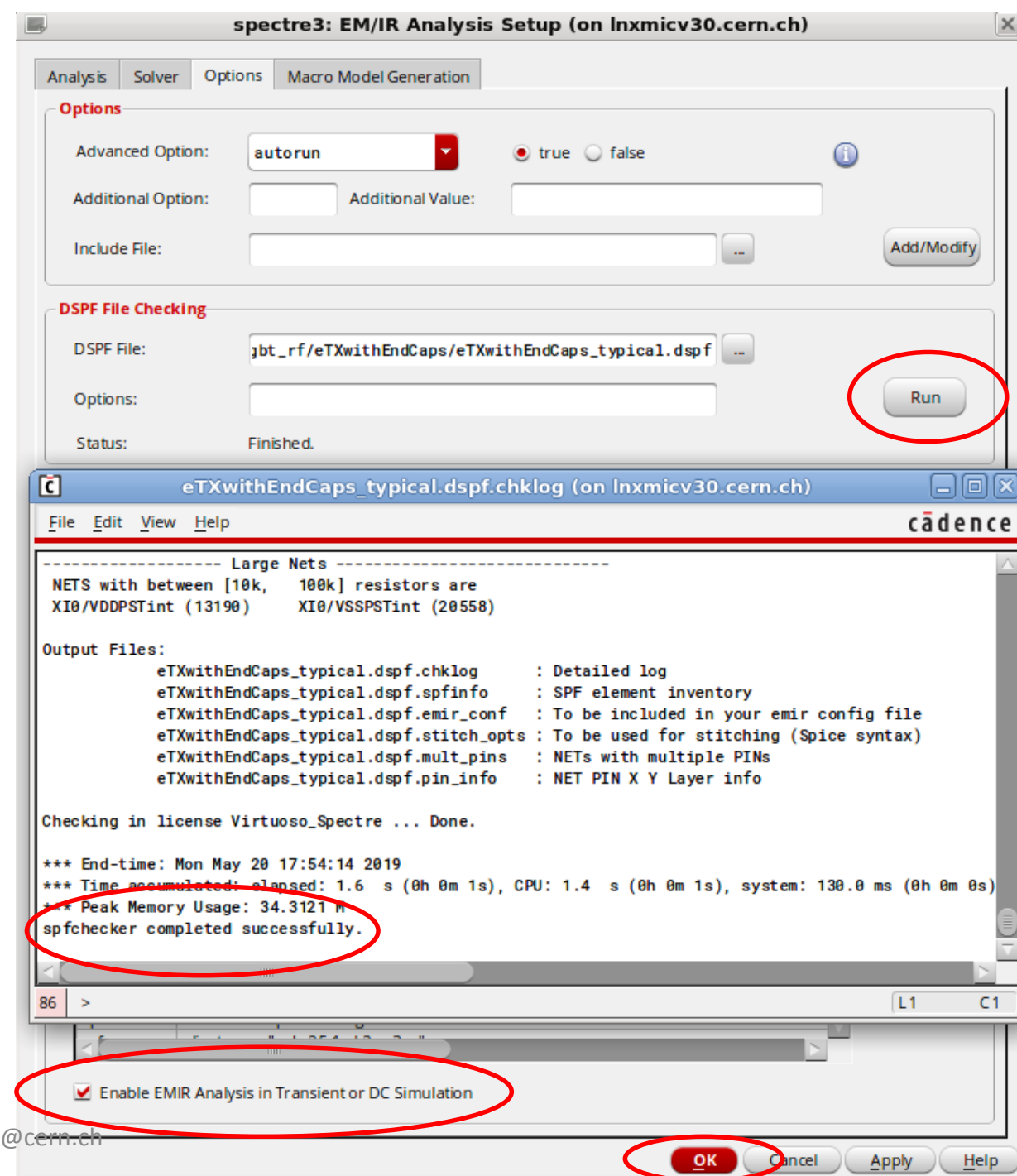
Run Simulation ADEXL Setup - Options

- Select “autorun”
- Add the adequate DSPF file, the same previously chosen in Simulation Files



Run Simulation ADEXL Setup - DSPF Checker

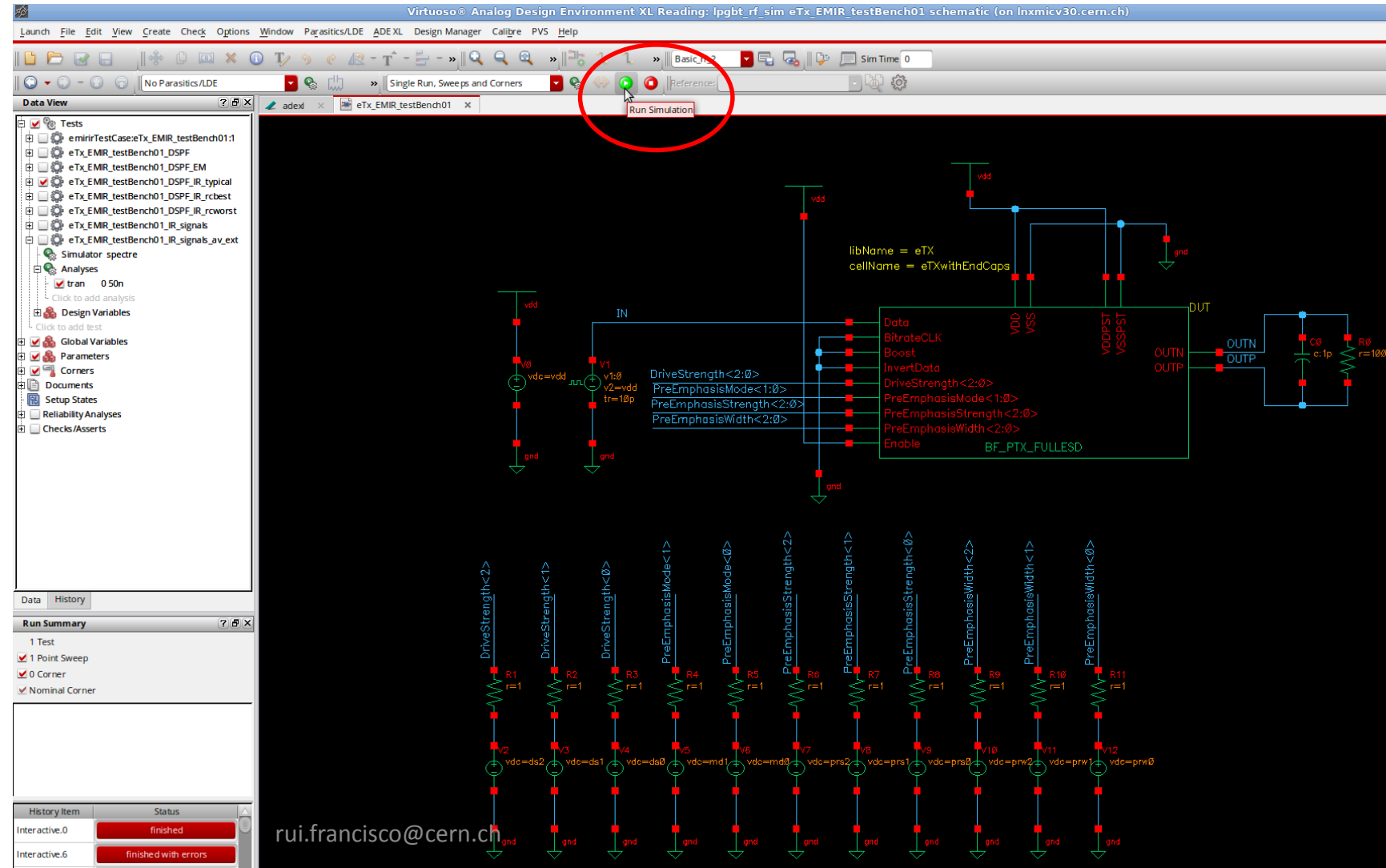
- Run the DSPF checker
- The checker should complete successfully
- Click “OK” after verifying that “Enable EMIR Analysis in Transient or DC Simulation” is ENABLED



Run Simulation ADEXL

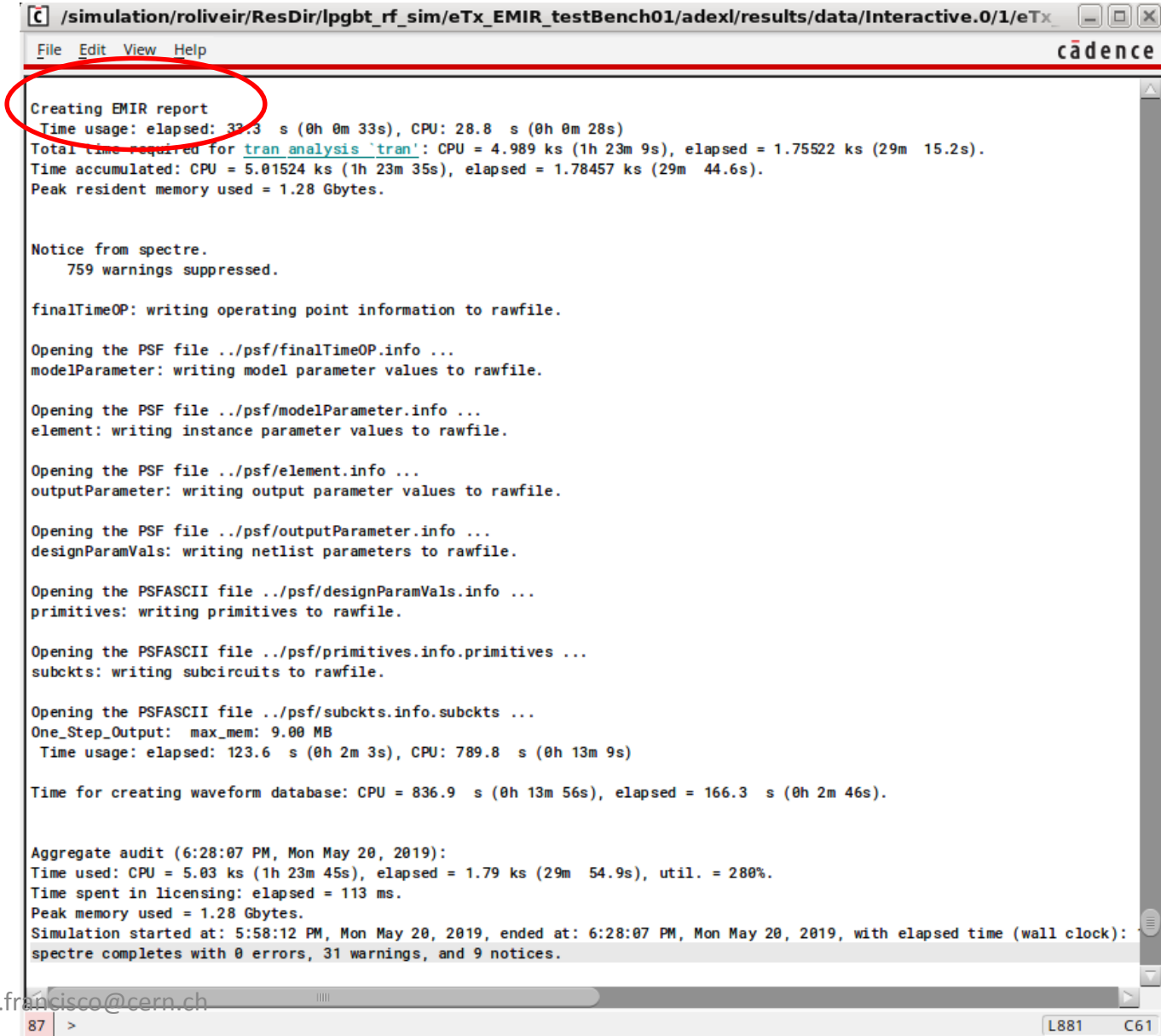
Run Simulation

- Run the Simulation



Run Simulation ADEXL EMIR Report

- Simulation log should show
“Creating EMIR report”



The screenshot shows a terminal window titled `/simulation/roliveir/ResDir/lpgbt_rf_sim/eTx_EMIR_testBench01/adexl/results/data/Interactive.0/1/eTx` with the Cadence logo in the top right corner. The menu bar includes `File Edit View Help`. The log content is as follows:

```
Creating EMIR report
Time usage: elapsed: 32.3 s (0h 0m 33s), CPU: 28.8 s (0h 0m 28s)
Total time required for tran analysis 'tran': CPU = 4.989 ks (1h 23m 9s), elapsed = 1.75522 ks (29m 15.2s).
Time accumulated: CPU = 5.01524 ks (1h 23m 35s), elapsed = 1.78457 ks (29m 44.6s).
Peak resident memory used = 1.28 Gbytes.

Notice from spectre.
759 warnings suppressed.

finalTimeOP: writing operating point information to rawfile.

Opening the PSF file ../psf/finalTimeOP.info ...
modelParameter: writing model parameter values to rawfile.

Opening the PSF file ../psf/modelParameter.info ...
element: writing instance parameter values to rawfile.

Opening the PSF file ../psf/element.info ...
outputParameter: writing output parameter values to rawfile.

Opening the PSF file ../psf/outputParameter.info ...
designParamVals: writing netlist parameters to rawfile.

Opening the PSFASCII file ../psf/designParamVals.info ...
primitives: writing primitives to rawfile.

Opening the PSFASCII file ../psf/primitives.info.primitives ...
subckts: writing subcircuits to rawfile.

Opening the PSFASCII file ../psf/subckts.info.subckts ...
One_Step_Output: max_mem: 9.00 MB
Time usage: elapsed: 123.6 s (0h 2m 3s), CPU: 789.8 s (0h 13m 9s)

Time for creating waveform database: CPU = 836.9 s (0h 13m 56s), elapsed = 166.3 s (0h 2m 46s).

Aggregate audit (6:28:07 PM, Mon May 20, 2019):
Time used: CPU = 5.03 ks (1h 23m 45s), elapsed = 1.79 ks (29m 54.9s), util. = 280%.
Time spent in licensing: elapsed = 113 ms.
Peak memory used = 1.28 Gbytes.
Simulation started at: 5:58:12 PM, Mon May 20, 2019, ended at: 6:28:07 PM, Mon May 20, 2019, with elapsed time (wall clock):
spectre completes with 0 errors, 31 warnings, and 9 notices.
```

The status bar at the bottom shows the file path `rui.francisco@cern.ch`, line `87`, and column `>`. The bottom right corner displays `L881 C61`.

Run Simulation ADEXL EMIR Log

- EMIR Analysis log can be checked with RMB over results in the Results tab, EM/IR Data, EM/IR Log

The image shows a Cadence Virtuoso window titled "Virtuoso® Analog Design Environment XL Editing: lpgbt_rf_sim eTx_EMIR_testBench01 adexl (on Inxmicv30.cern.ch)". The window has a menu bar (Launch, File, Create, Tools, Options, Run, EAD, Parasitics/LDE, Window, Calibre, Help) and a toolbar. Below the toolbar, there are tabs for "Data View" and "Results". The "Data View" tab is active, showing a tree structure of tests and analyses. The "Results" tab is also visible, showing a table of test results. A right-click context menu is open over the "Results" tab, showing options like "Output Log", "View Netlist", "View Netlisted Checks/Asserts", "View Dynamic/Static Violation Report", "Open Terminal ...", "Job Log", "Cancel Selected Simulation(s)", "Plot All", "Plot", "Quick Plot All", "Plot Across Corners", "Plot Across Design Points", "Create Copy Of Selected Corner", "Troubleshoot Point", "Open Debug Environment ...", "Open Results Browser ...", "Open Calculator ...", "Plot Outputs", "Direct Plot", "Print", "Annotate", "Annotation Balloons", "Vector", "Circuit Conditions ...", "Reliability Data", "EM/IR Data", "EM/IR Log", "Add to Spec Summary", and "Customize Menus...". The "EM/IR Log" option is highlighted with a red circle.

The "Results" tab shows a table with the following columns: Test, Output, Nominal, Spec, Weight, Pass/Fail. The table contains three rows of test results:

Test	Output	Nominal	Spec	Weight	Pass/Fail
eTx_EMIR_testBench01_DSPF_IR_typical	/DUT/0017/net014				
eTx_EMIR_testBench01_DSPF_IR_rcbest	(VT("/OUTP") - VT("/OUTN"))				
eTx_EMIR_testBench01_DSPF_IR_typical	eyeDiagram(VT("/OUTP") - VT("/OUTN"))				

The "Data View" tab shows a tree structure of tests and analyses. The tree is expanded to show the "Analyses" section, which includes "tran 0.50n".

The bottom window shows the command line output of the simulation. The output includes the following information:

```
INFO: Starting Voltus-Fi Batch Mode Application.

Command run is:
*****
/eda/cadence/2017-18/RHELx86/SPECTRE_16.10.510/tools.lnx86/sev/bin/64bit/emirreport -c /simulation/roliveir/ResDir/lpgbt
*****

Voltus-Fi version being used is as follows:
*****
Voltus-Fi batch mode application (64-bit) - High Capacity Power IR/EM - v06.17-e460_1 ((09/01/2017 04:10:14))
-----
Copyright (c) Cadence Design Systems, Inc. 1996 - 2014
*****

INFO: loading MMSIM results
INFO: loading MMSIM all net results
INFO: Running EM on all nets
Starting EM all nets
```

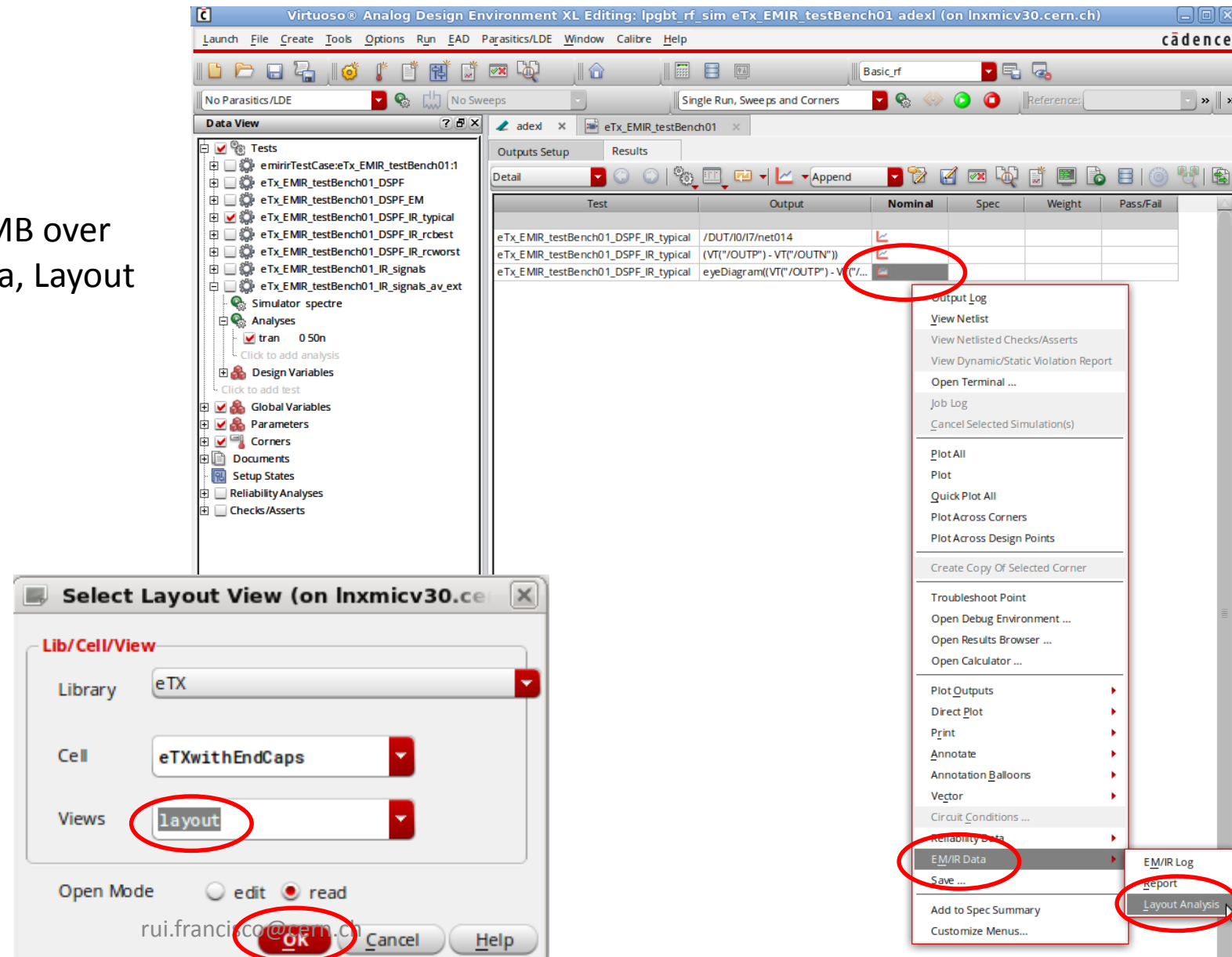

EMIR Analysis Layout Analysis

- To show the results in the layout, RMB over results in the Results tab, EM/IR Data, Layout Analysis

- Select the cell layout view

- Click "OK"

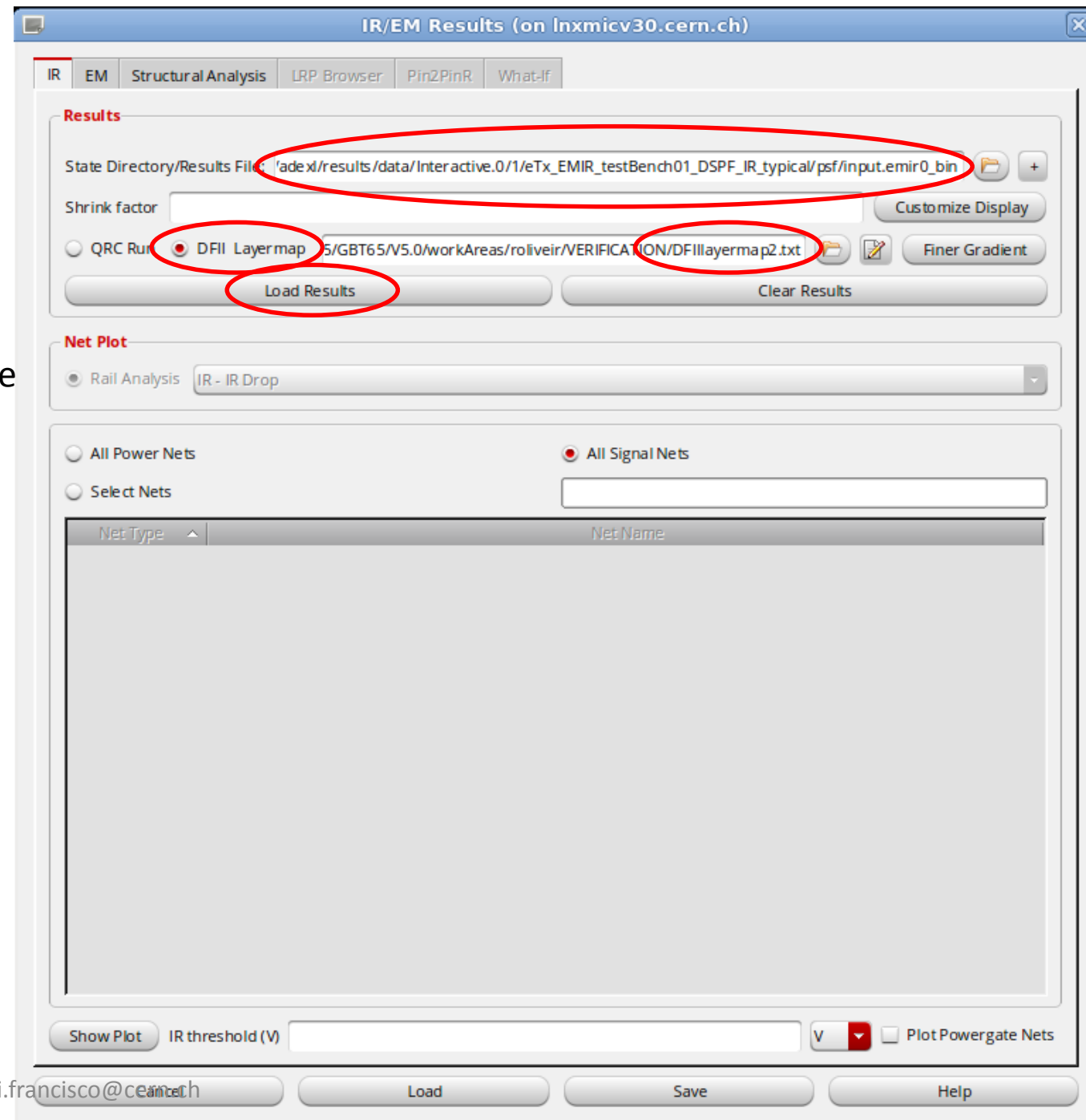
20/05/2019



EMIR Analysis

IR - Load Results

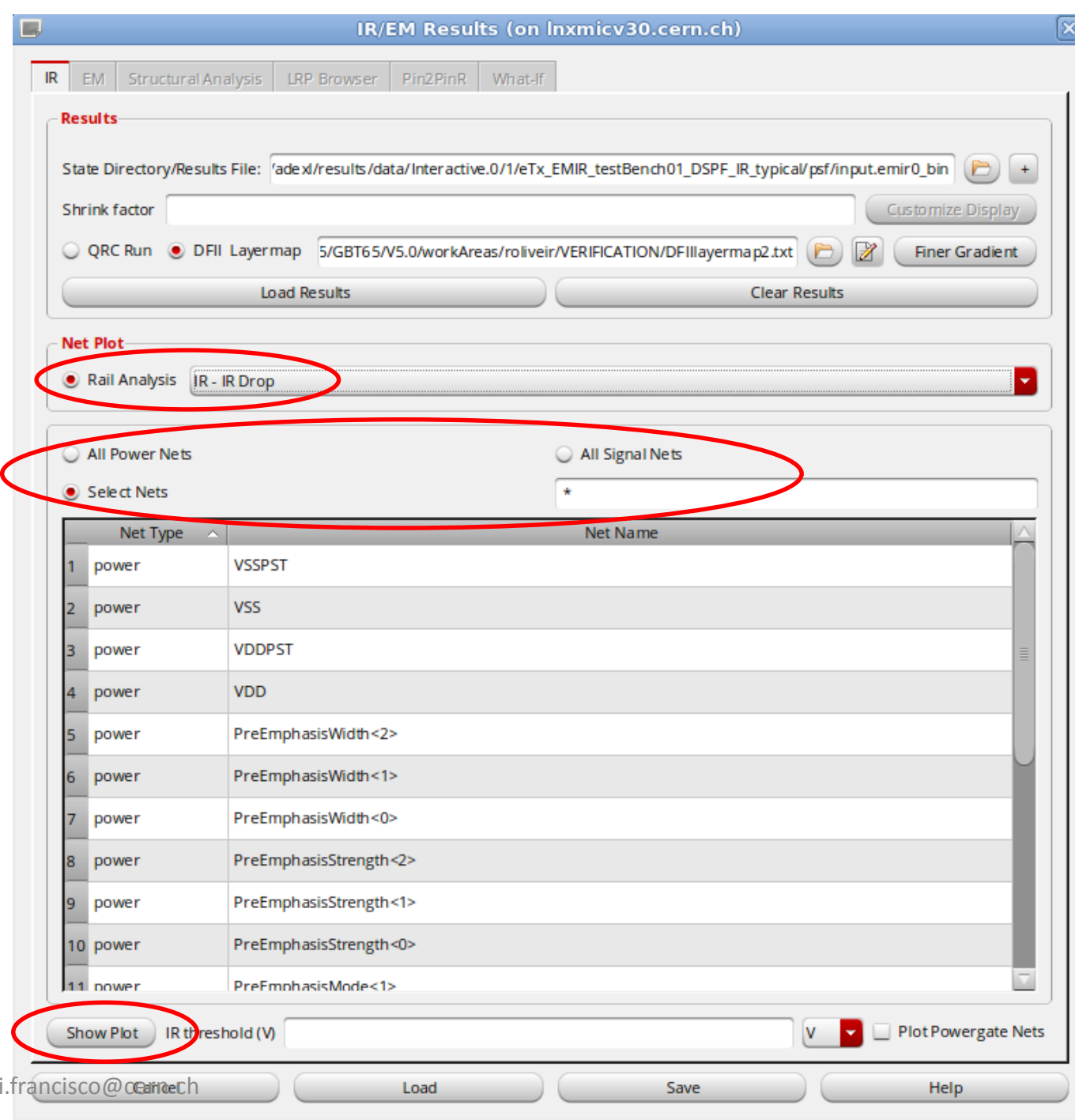
- Browse for and Select the “input.emir0_bin” file in the simulation results folder
 - /(simulation path)/ResDir/ (design library)
/(cell name) /adexl/results/data
/(Interactive name)/1/ (test name)
/psf/input.emir0_bin
- Select DFII Layermap
- Browse for and Select DFII layermap file
- Click “Load Results”



EMIR Analysis

IR - Rail Analysis

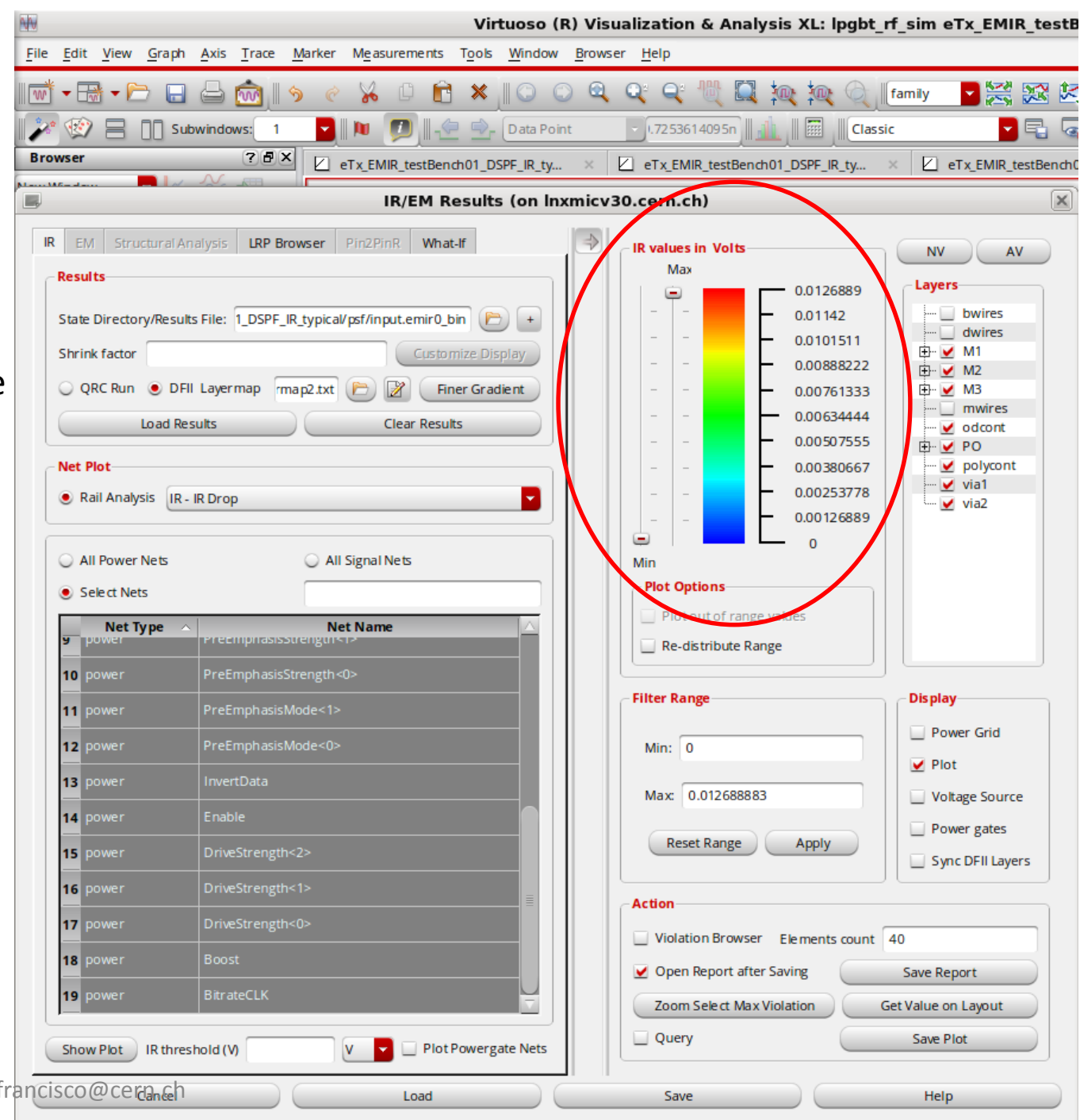
- Choose Rail Analysis type
 - IR - IR Drop :peak values
 - IRAVG - IR Avg Drop: average values
- Select Nets and/or type of Nets
- Click “Show Plot”



EMIR Analysis

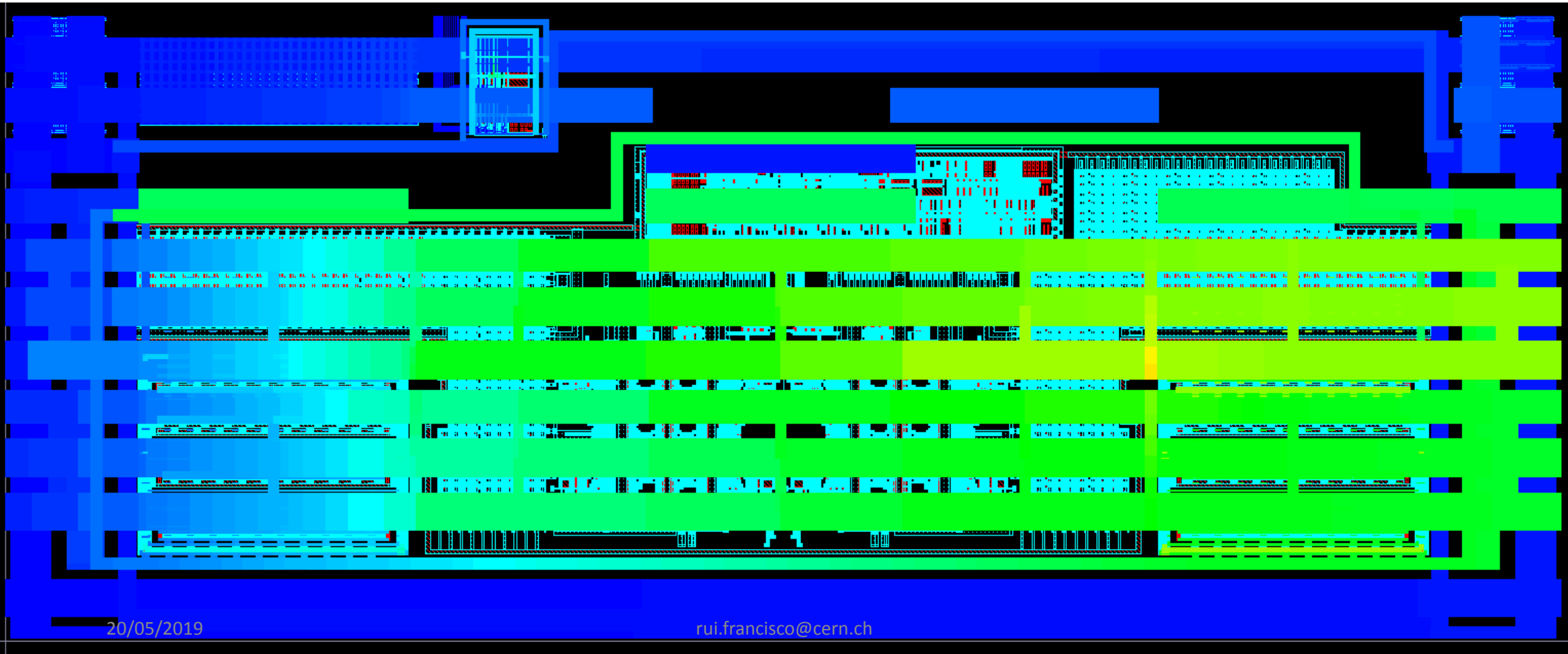
IR - Power Nets

- “IR values in Volts” shows the voltage drop scale
- The “Action” panel can be used to find violations / maximum values



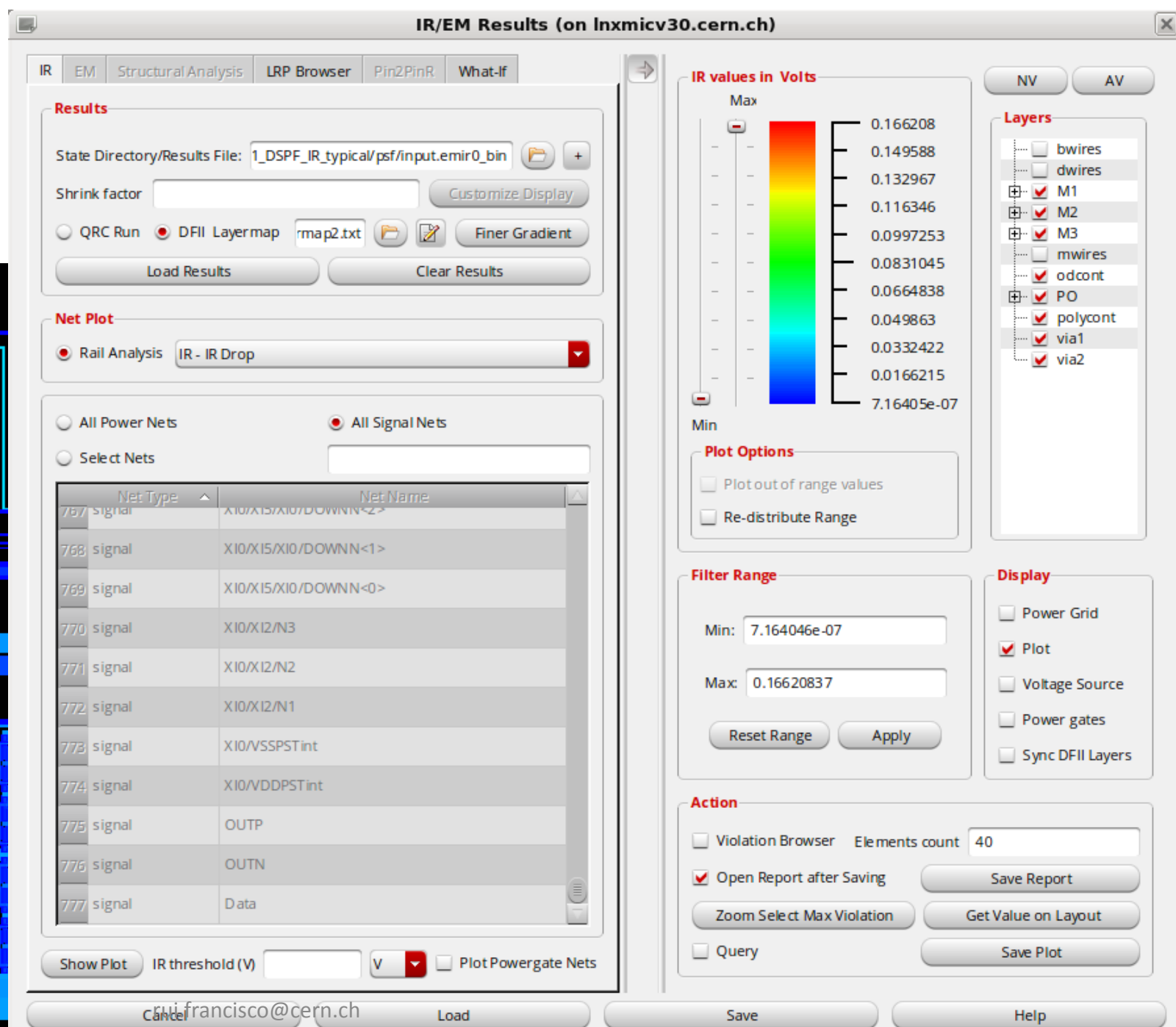
EMIR Analysis

IR - Power Nets



EMIR Analysis

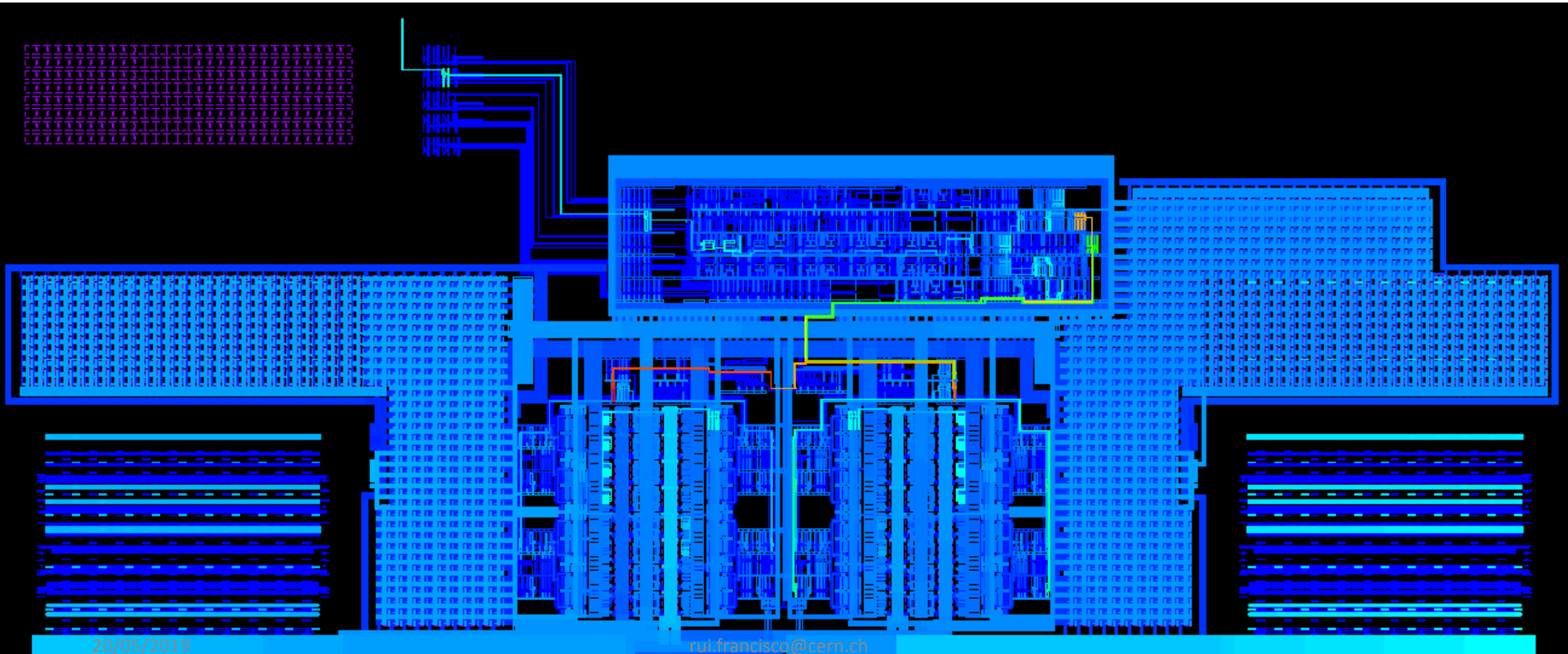
IR - Signal Nets



20/05/2019

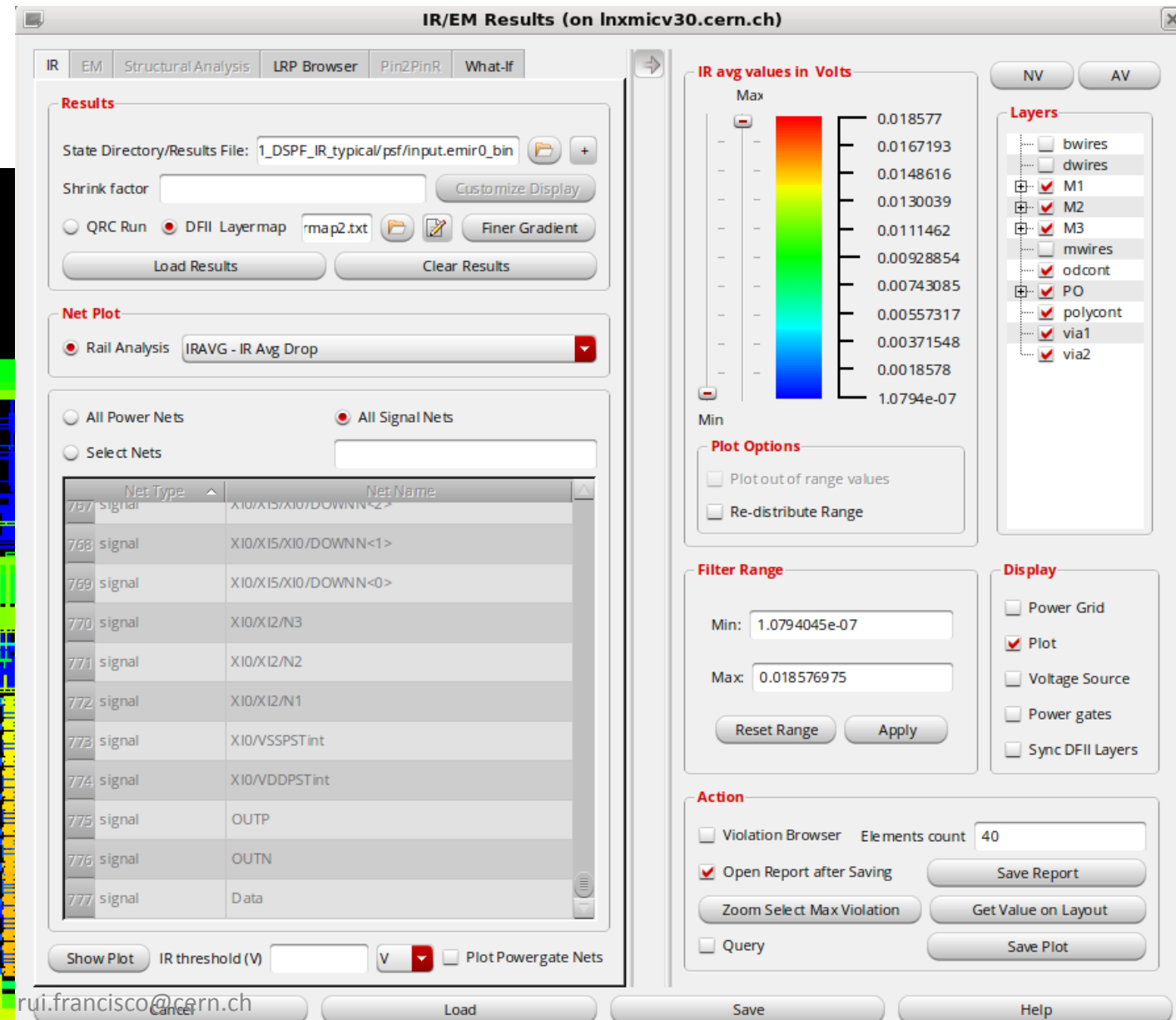
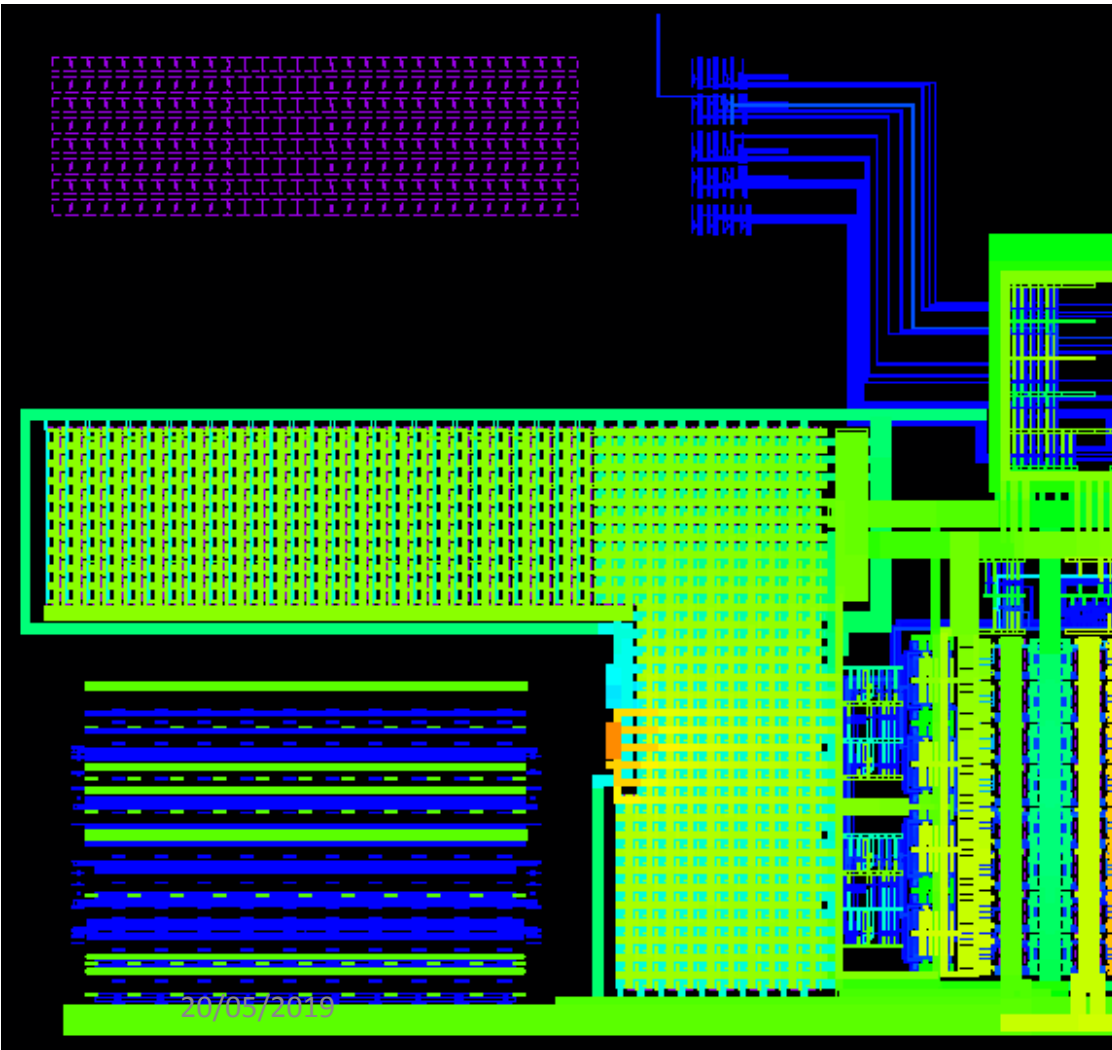
EMIR Analysis

IR - Signal Nets



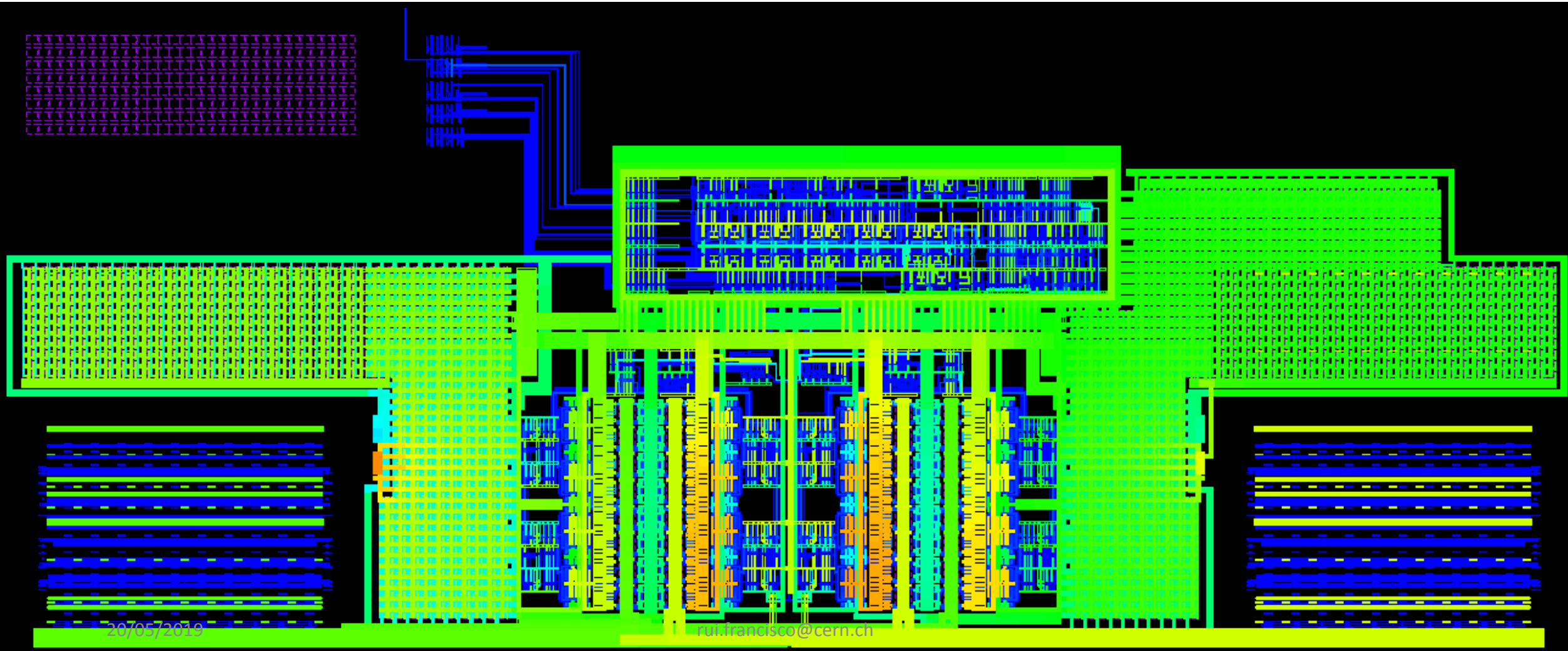
EMIR Analysis

IR AVG - Signal Nets



EMIR Analysis

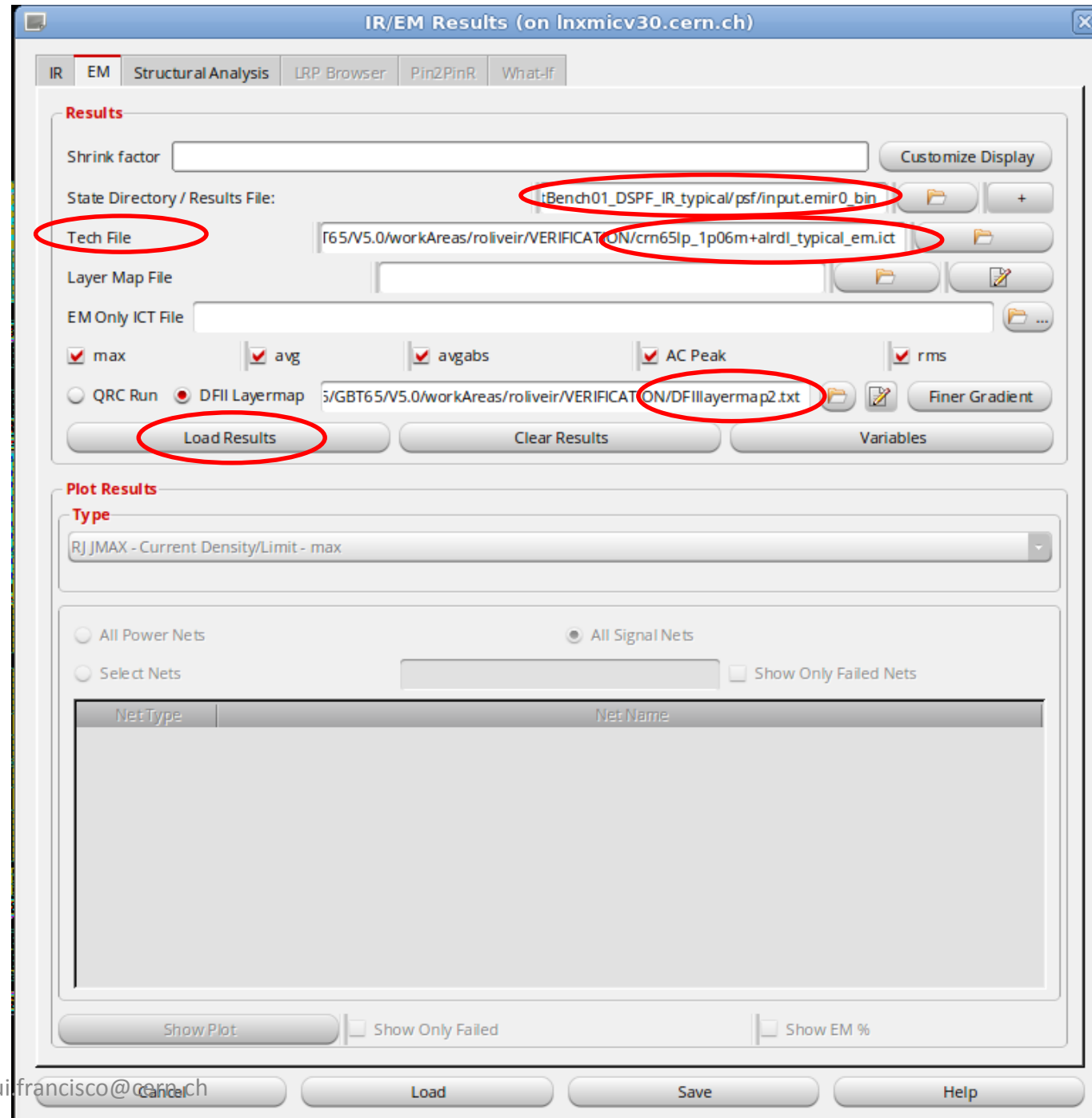
IR AVG - Signal Nets



EMIR Analysis

EM - Load Results

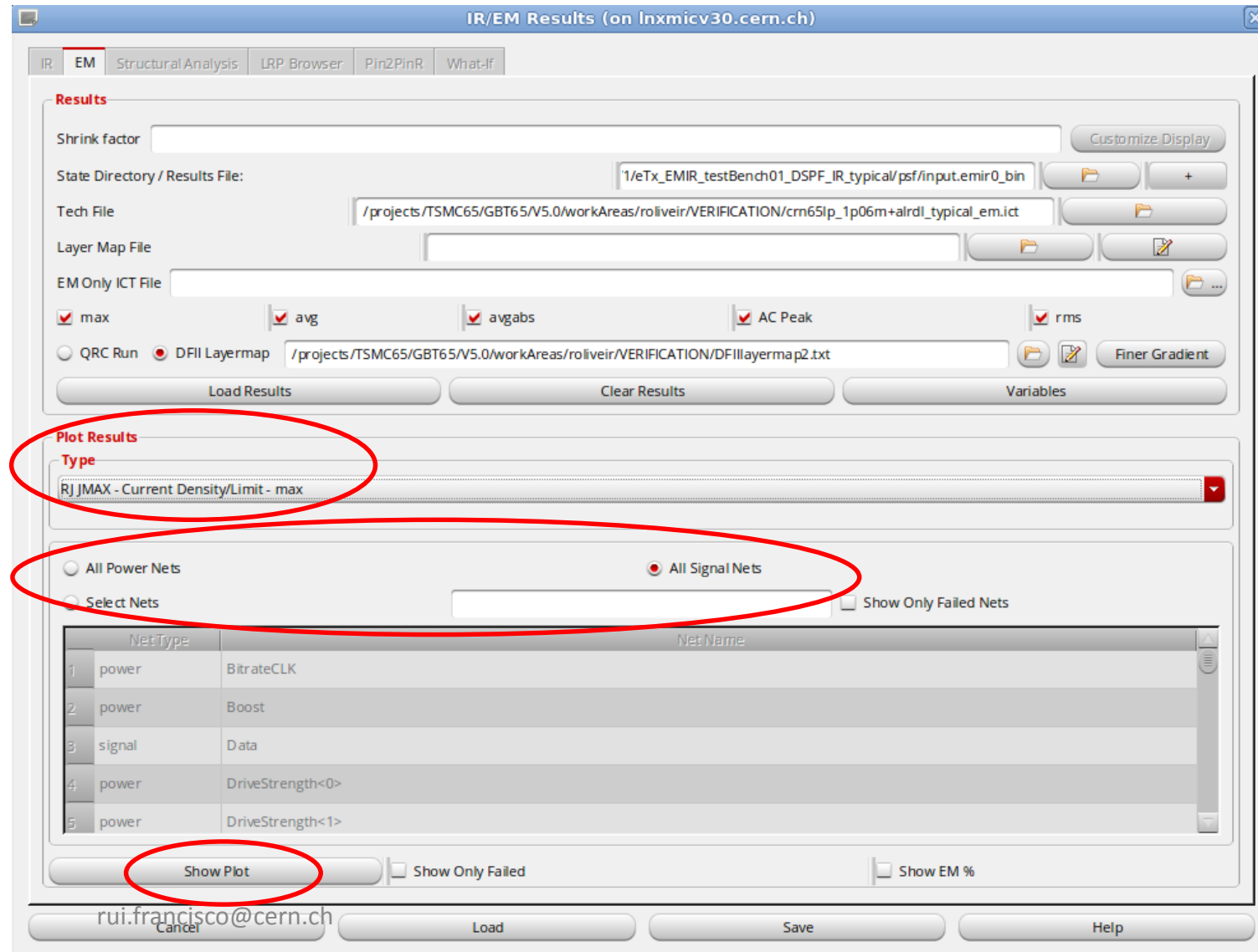
- Browse for and Select the “input.emir0_bin” file in the simulation results folder
 - /(simulation path)/ResDir/ (design library) /(cell name) /adexl/results/data /(Interactive name)/1/ (test name) /psf/input.emir0_bin
- Add the previously used “*_em.ict” Tech File
- Select DFII Layermap
- Browse for and Select DFII layermap file
- Click “Load Results”



EMIR Analysis

EM - Type

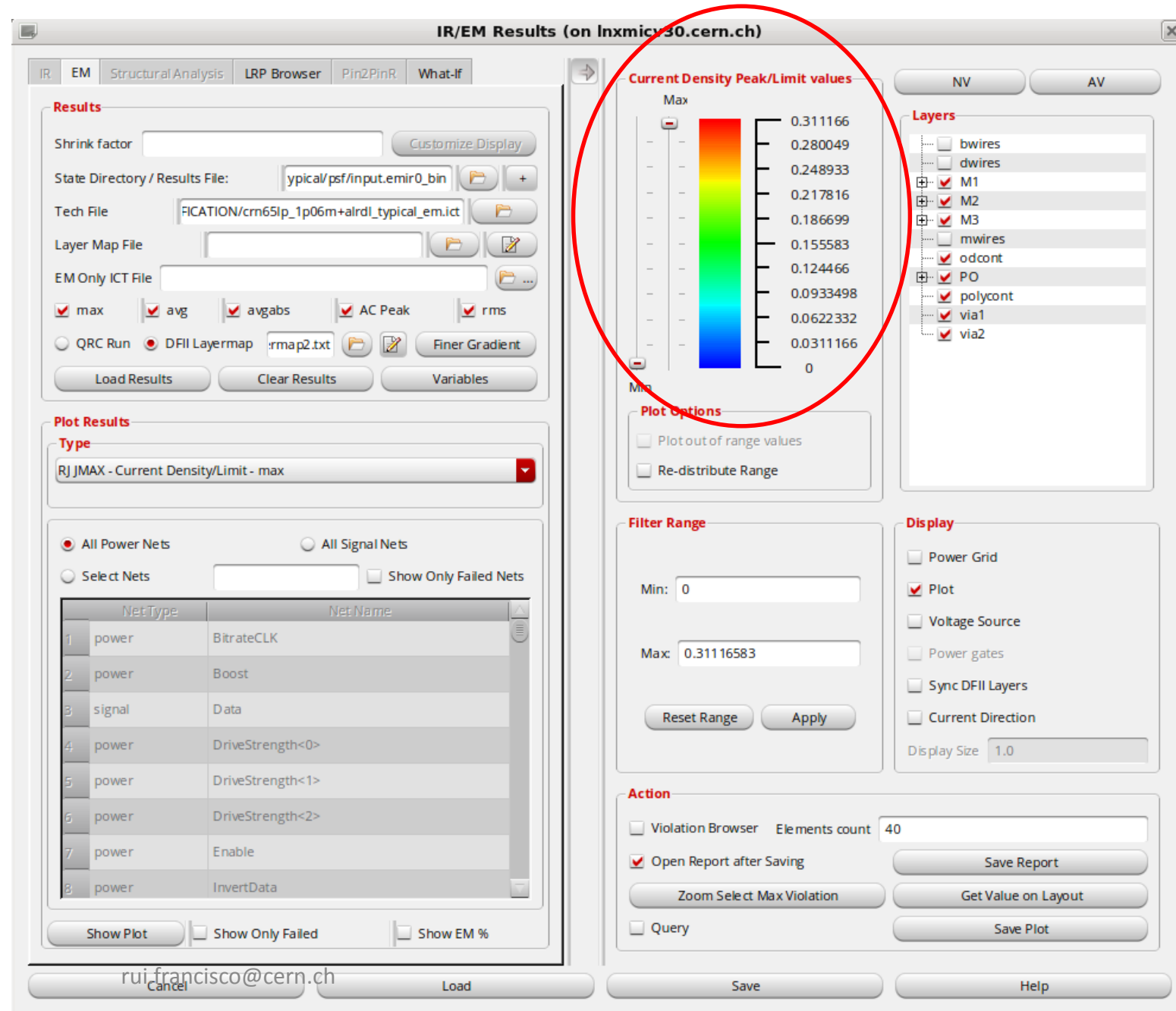
- Choose Plot Results type
 - RJ JMAX - Current Density / Limit
- Select Nets and/or type of Nets
- Click “Show Plot”



EMIR Analysis

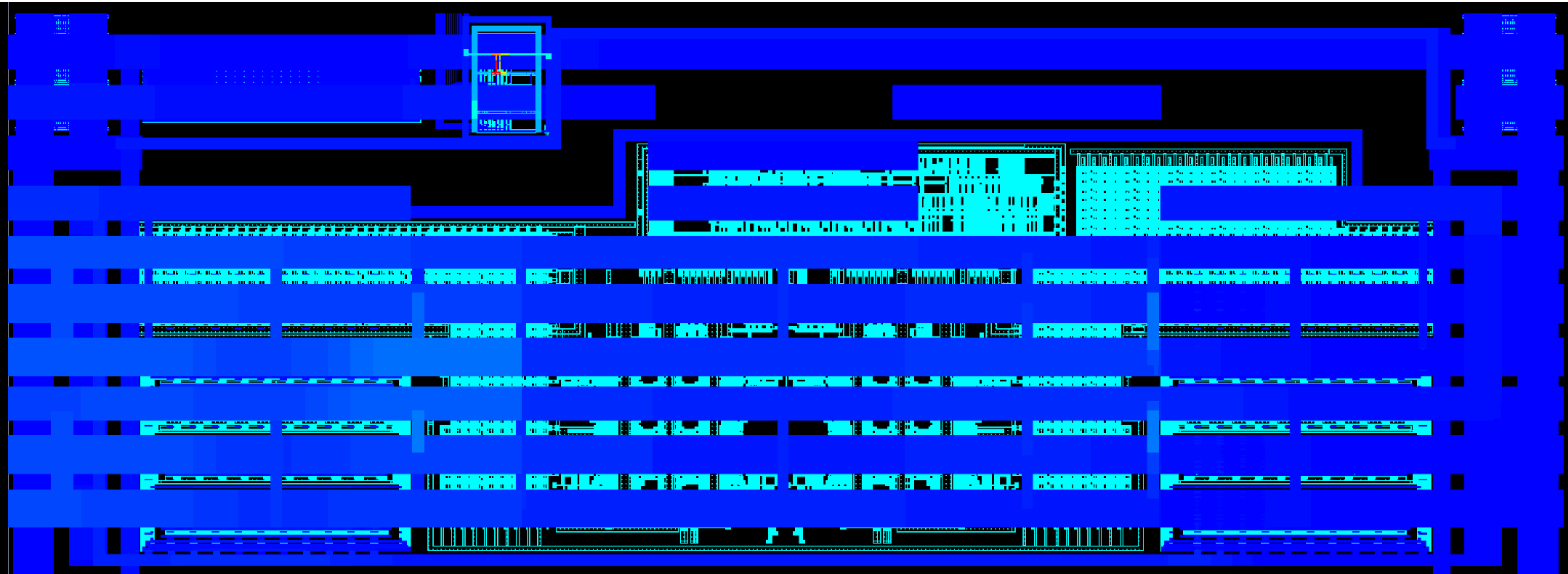
EM - Power Nets

- “Current Density Peak/Limit values” shows the ratio of current capability used
- In this example 31% of the path current capability is being used
- The “Action” panel can be used to find violations / maximum values
- If selecting the “Show EM %”, the “Save Report” can show false failing situations due to a bug in current density calculation



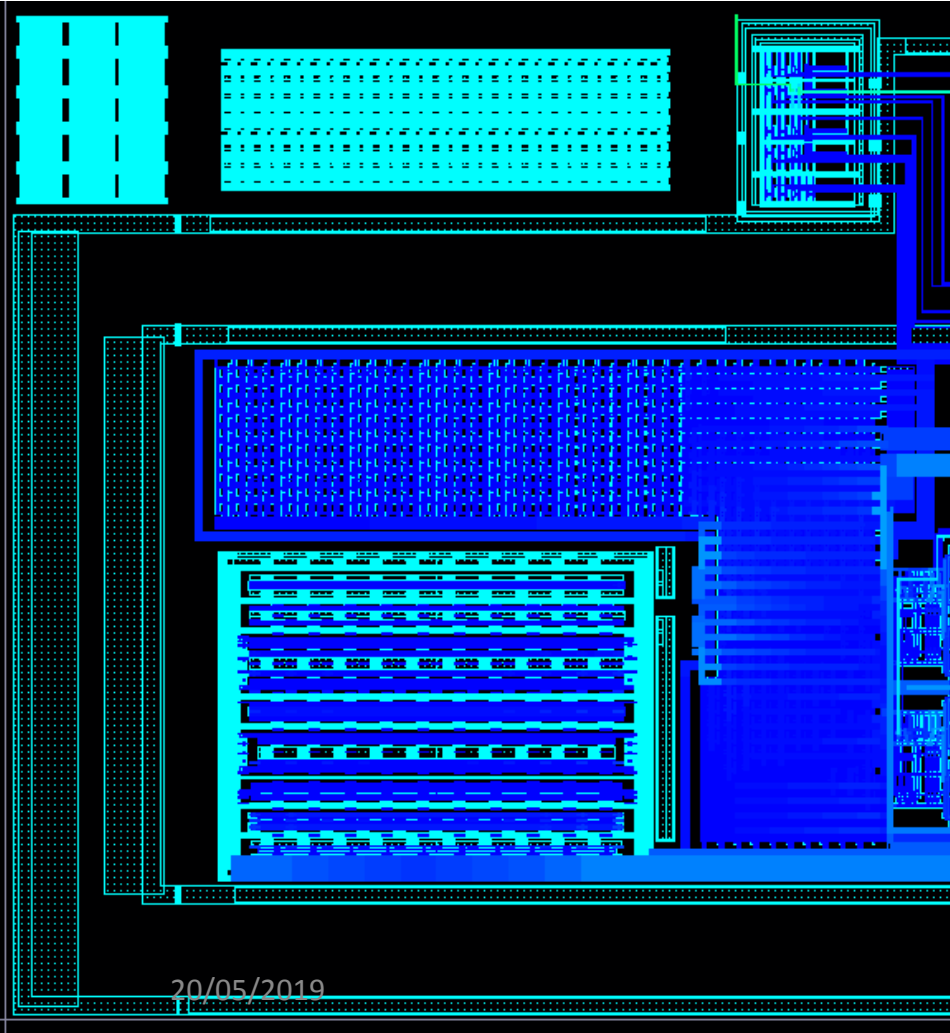
EMIR Analysis

EM - Power Nets



EMIR Analysis

EM - Signal Nets



IR/EM Results (on Inxmicv30.cern.ch)

IR EM Structural Analysis LRP Browser Pin2PinR What-If

Results

Shrink factor [Customize Display](#)

State Directory / Results File: [+](#)

Tech File [+](#)

Layer Map File [+](#) [✎](#)

EM Only ICT File [+](#)

☒ max ☒ avg ☒ avgabs ☒ AC Peak ☒ rms

☐ QRC Run ☒ DFII Layermap [+](#) [✎](#) [Finer Gradient](#)

[Load Results](#) [Clear Results](#) [Variables](#)

Plot Results

Type [v](#)

☐ All Power Nets ☒ All Signal Nets

☐ Select Nets ☐ Show Only Failed Nets

	Net Type	Net Name
1	power	BitrateCLK
2	power	Boost
3	signal	Data
4	power	DriveStrength<0>
5	power	DriveStrength<1>
6	power	DriveStrength<2>
7	power	Enable
8	power	InvertData

[Show Plot](#) ☐ Show Only Failed ☐ Show EM %

[Cancel](#) [Load](#)

Current Density Peak/Limit values

Max 0.86043
0.774387
0.688344
0.602301
0.516258
0.430215
0.344172
0.258129
0.172086
0.086043
Min 0

Plot Options

☐ Plot out of range values
☐ Re-distribute Range

Filter Range

Min:
Max:
[Reset Range](#) [Apply](#)

Display

☐ Power Grid
☒ Plot
☐ Voltage Source
☐ Power gates
☐ Sync DFII Layers
☐ Current Direction
Display Size

Action

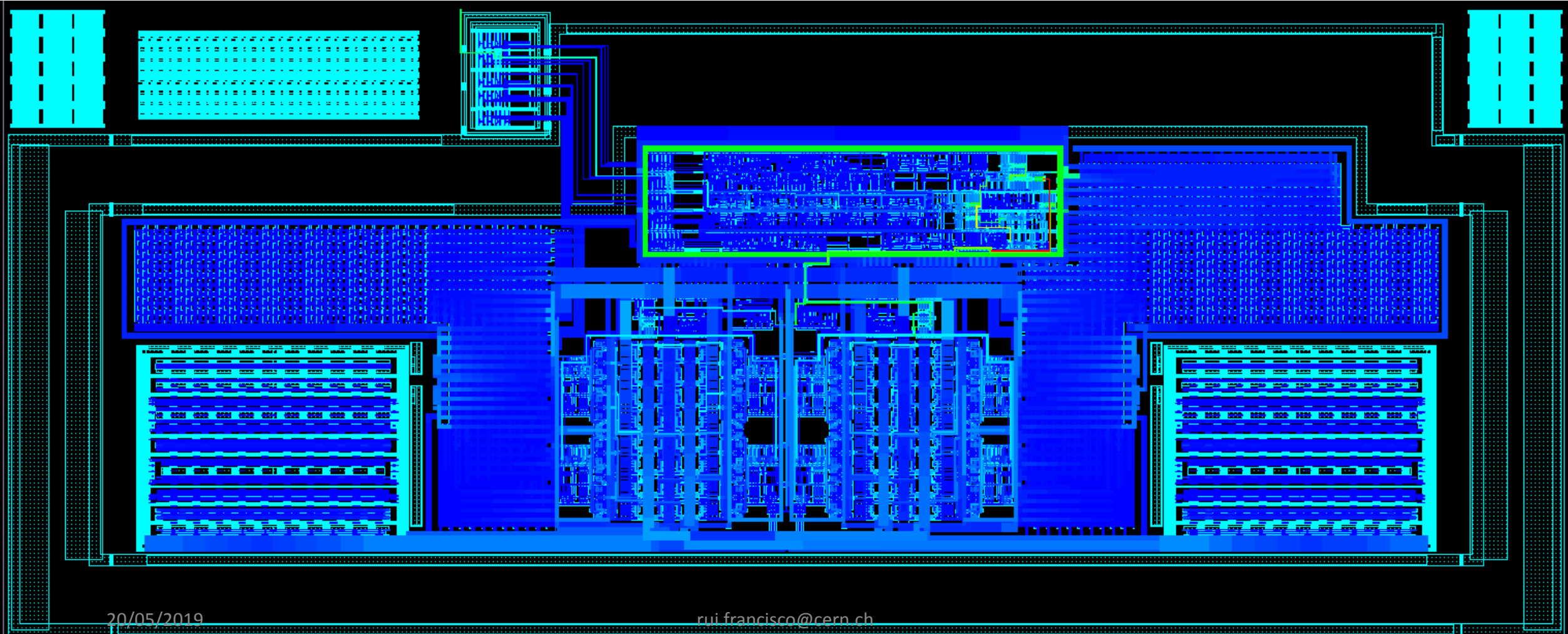
☐ Violation Browser Elements count
☒ Open Report after Saving [Save Report](#)
[Zoom Select Max Violation](#) [Get Value on Layout](#)
☐ Query [Save Plot](#)

[Save](#) [Help](#)

rui.francisco@cern.ch

EMIR Analysis

EM - Signal Nets



The End

APPENDIX

pvtech.lib

```
-- DEFINE tsmc65n $PDK_PATH/V1.7A_1/$OPTION/PVS_QRC  
DEFINE tsmc65n ./PVS_QRC
```

crn65lp_1p06m+alrdl_typical_em.ict

```
#####  
##### ICT File Generated by ircxtoict -em_update  
##### ircxtoict Release : 15.2.1-s070  
##### IRCXTOICT Control ID : 2.52  
##### Input IRCX File : RC_IRCX_CLN65LP_1P6M+ALRDL_3X2Z_typical.ircx  
##### Input IRCX File version : V1.5a ##### Input ICT File : crn65lp_1p06m+alrdl_typical.ict  
##### Output ICT File : crn65lp_1p06m+alrdl_typical_em.ict  
#####  
process "crn65lp_1p06m+alrdl_typical" {  
...  
}
```

Dfllayermap2.txt

#<type> <extraction_layer_name> <dfll_layer_name>

metal	metal1	M1
metal	metal2	M2
metal	metal3	M3
metal	metal4	M4
metal	metal5	M5
metal	metal6	M6
metal	metal7	AP
poly	poly	PO
od	od	OD
via	odCont	CO
via	via1	VIA1
via	via2	VIA2
via	via3	VIA3
via	via4	VIA4
via	via5	VIA5
via	via6	RV

rnpolys_sub_circuit.spi

- ++++++ *
- * Sub cell: rnpolys *
- * ++++++ *
- .subckt rnpolys PLUS MINUS
- .ends rnpolys

References

- IC6.1.7: Voltus-Fi EMIR Analysis Workshop- The DSPF flow:

<https://support.cadence.com/apex/articleattachmentportal?id=a1O0V000009ETFdUAO&pageName=ArticleContent&attachId=0690V000004Z7ypQAC&sq=null>

- Voltus-Fi-L EMIR Analysis Workshop - Extracted View Flow:

<https://support.cadence.com/apex/ArticleAttachmentPortal?id=a1O0V000007MnyIUAC&pageName=ArticleContent>

- EM models from Cadence support how to:

https://community.cadence.com/cadence_blogs_8/b/di/posts/five-minute-tutorial-creating-an-em-model-file

https://community.cadence.com/cadence_blogs_8/b/di/posts/five-minute-tutorial-em-model-files-revisited

https://community.cadence.com/cadence_blogs_8/b/di/posts/five-minute-tutorial-one-more-look-at-em-models