# VOLTUS-FI

EMIR PVS Flow

Step-by-Step

by

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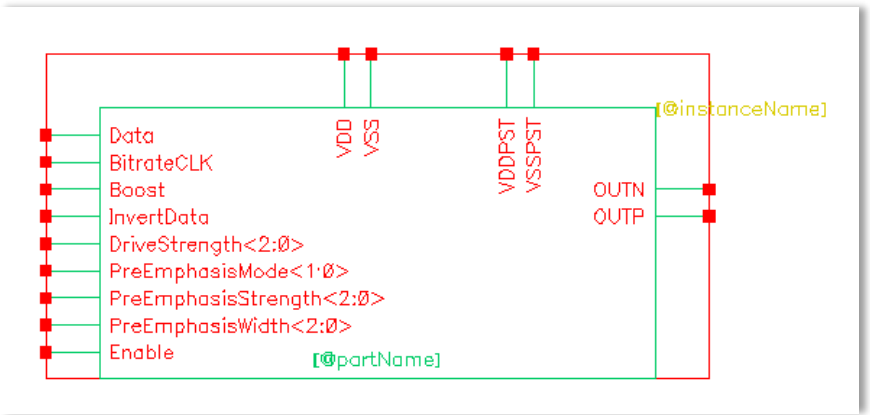
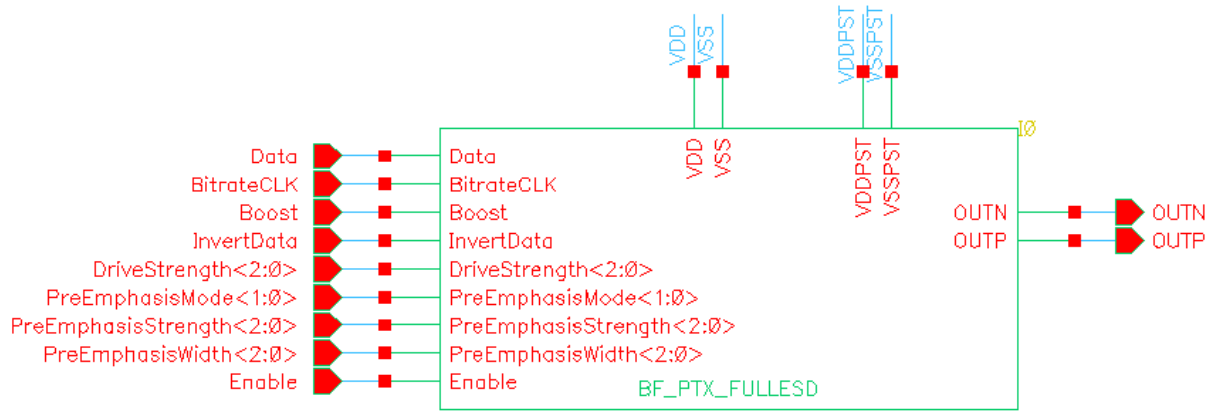
# Requirements

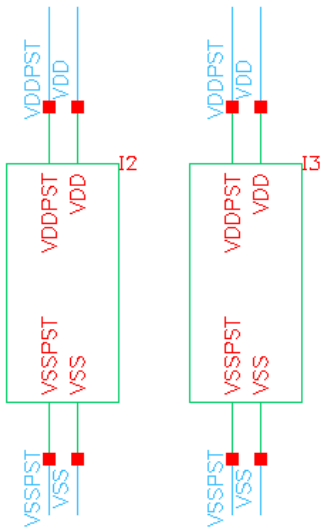
- VOLTUS-FI installed
- Files (check appendix):
  - Technology mapping file: pvtech.lib
  - PVS_QRC rules files for typical, best and worst cases
  - Electromigration models files for typical, best and worst cases
    - crn65lp_1p06m+alrdl_typical_em.ict
    - crn65lp_1p06m+alrdl_rcbest_em.ict
    - crn65lp_1p06m+alrdl_rcworst_em.ict
  - DFII layermap file: DFIIlayermap2.txt
  - Empty sub-circuit netlist files for devices without models
    - rnpolys_sub_circuit.spi, rnpolywo_m_sub_circuit.spi

# Create Schematic and Symbol







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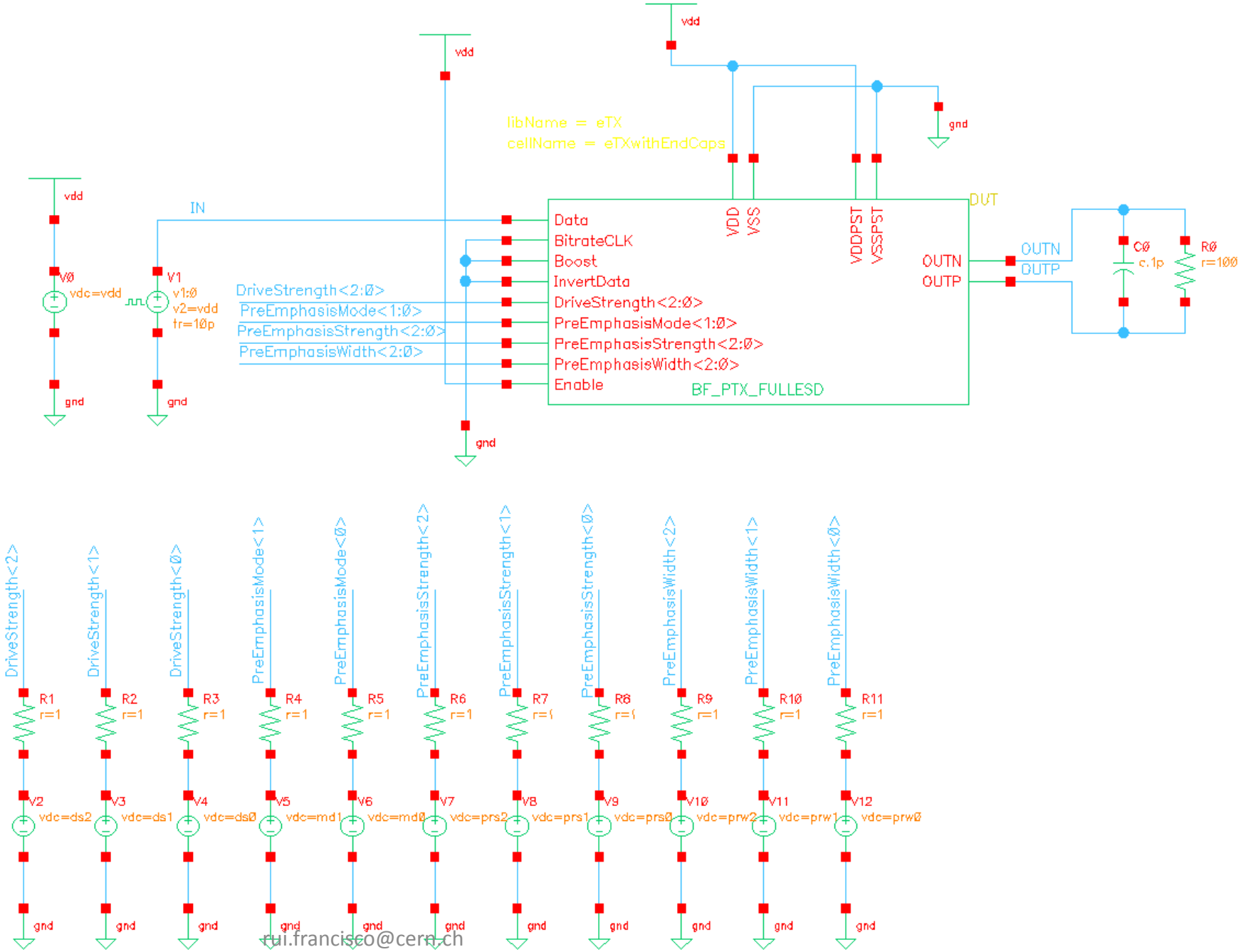
# Create Test Bench





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# And Simulate

- Use ADEXL to setup schematic simulation



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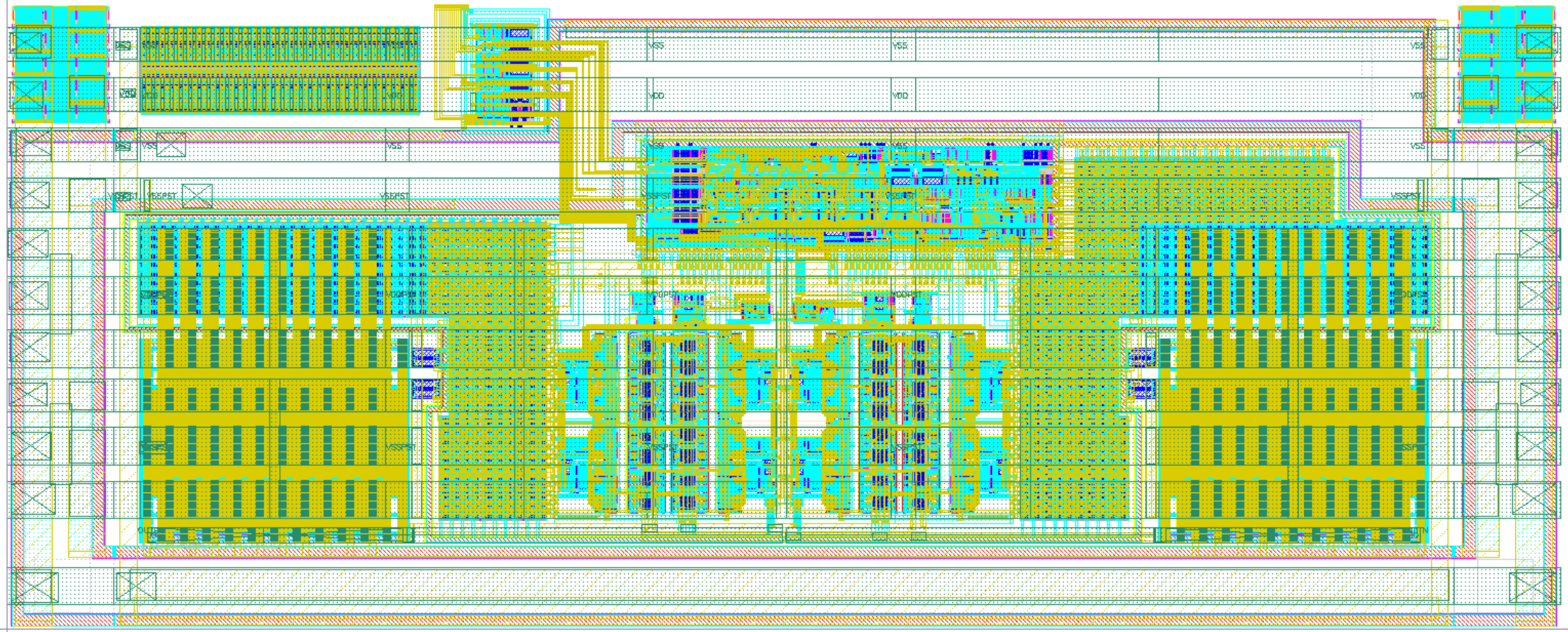
# Create Layout





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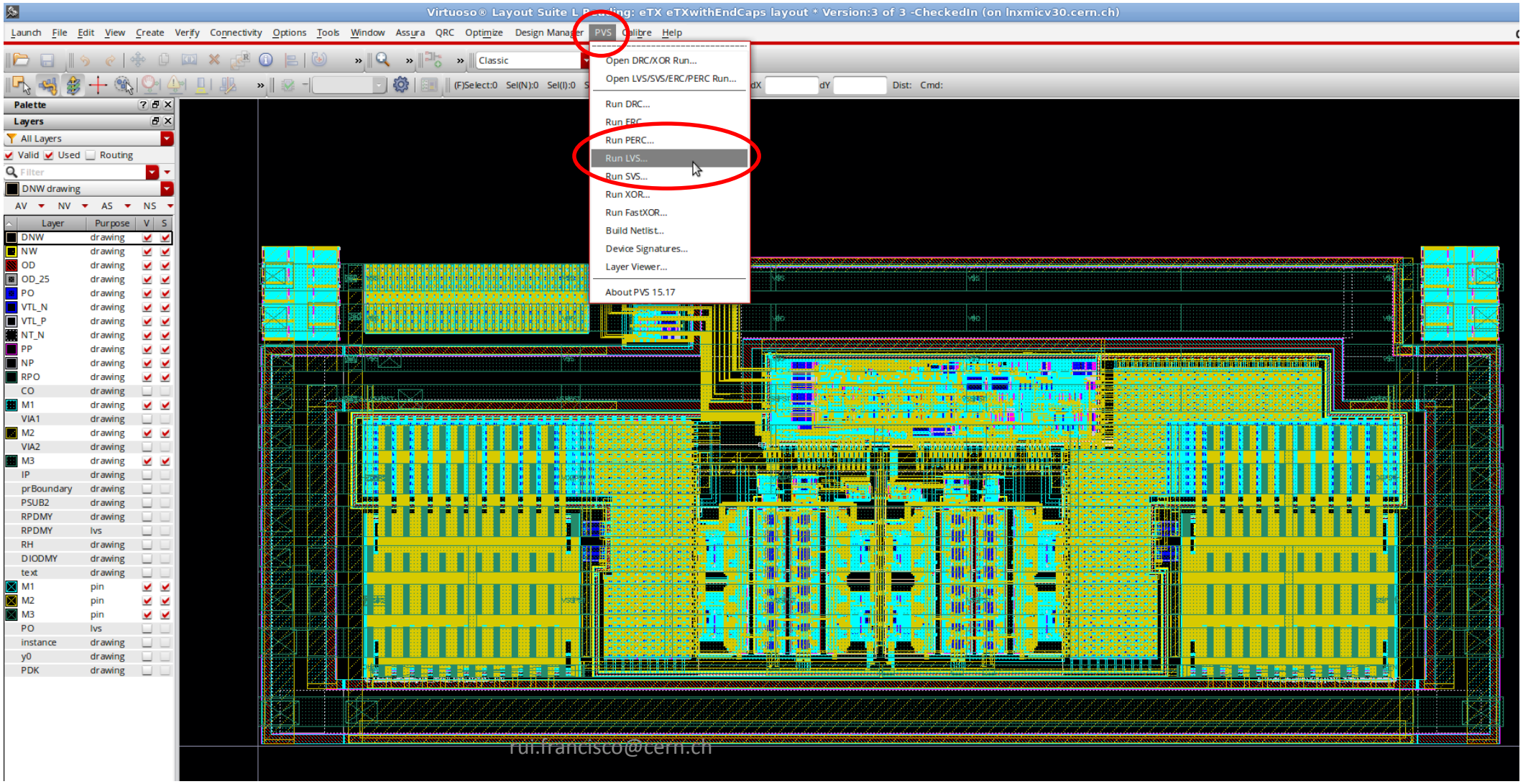
# Run LVS using PVS
# Virtuoso - Menu





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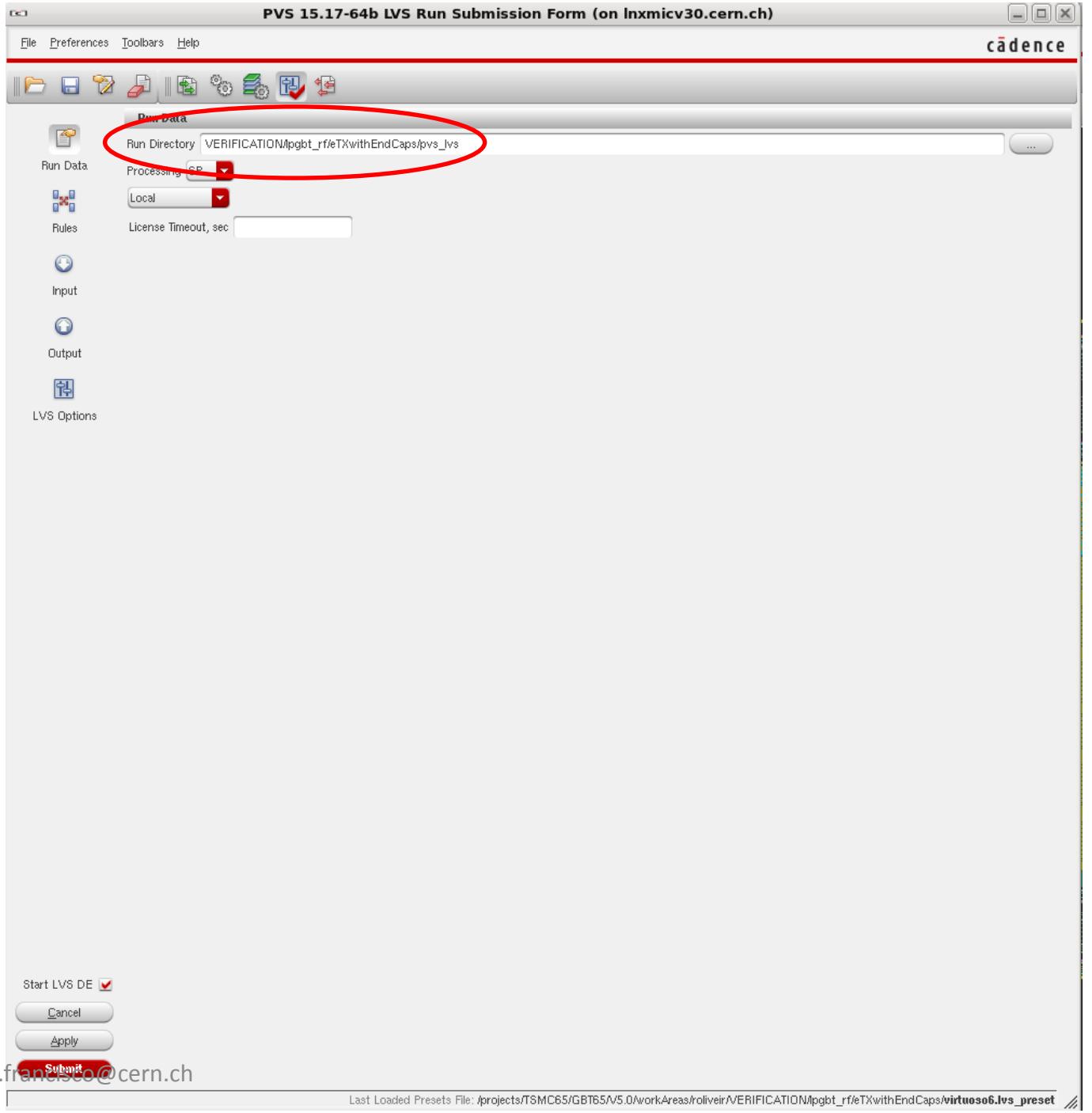
# Run LVS using PVS Setup - Run Data

- Setup “Run Directory”



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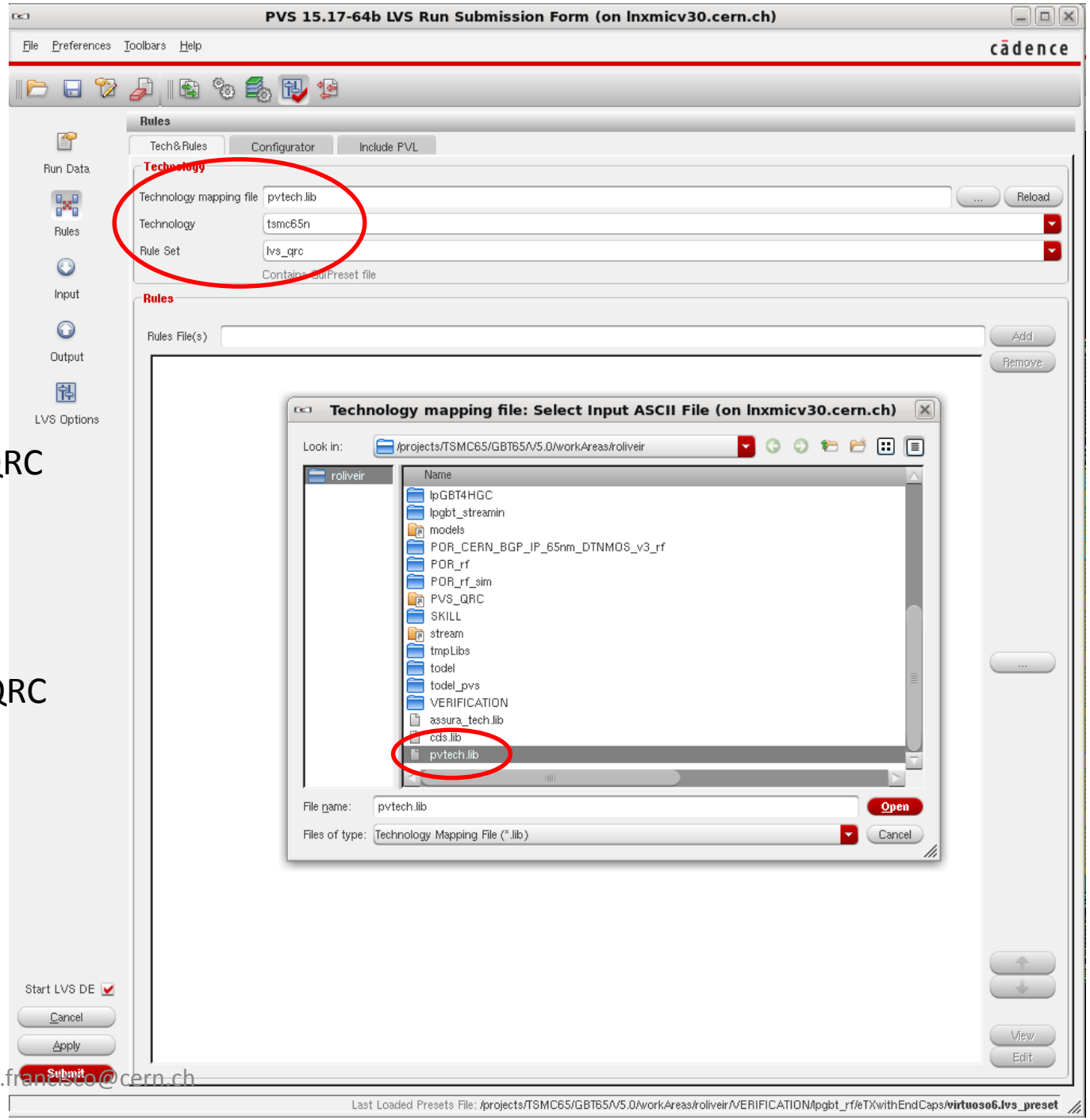
# Run LVS using PVS Setup - Rules

- Find and select “pvtech.lib” file
- “pvtech.lib” file contains the path to the PVS_QRC technology/configuration files:
  “DEFINE tsmc65n ./PVS_QRC”
- ./PVS_QRC is a link to:
  (TSMC65 installation path)/1p6m3x1z1u/PVS_QRC
- Select Technology: tsmc65n
- Select Rule Set: lvs_qrc





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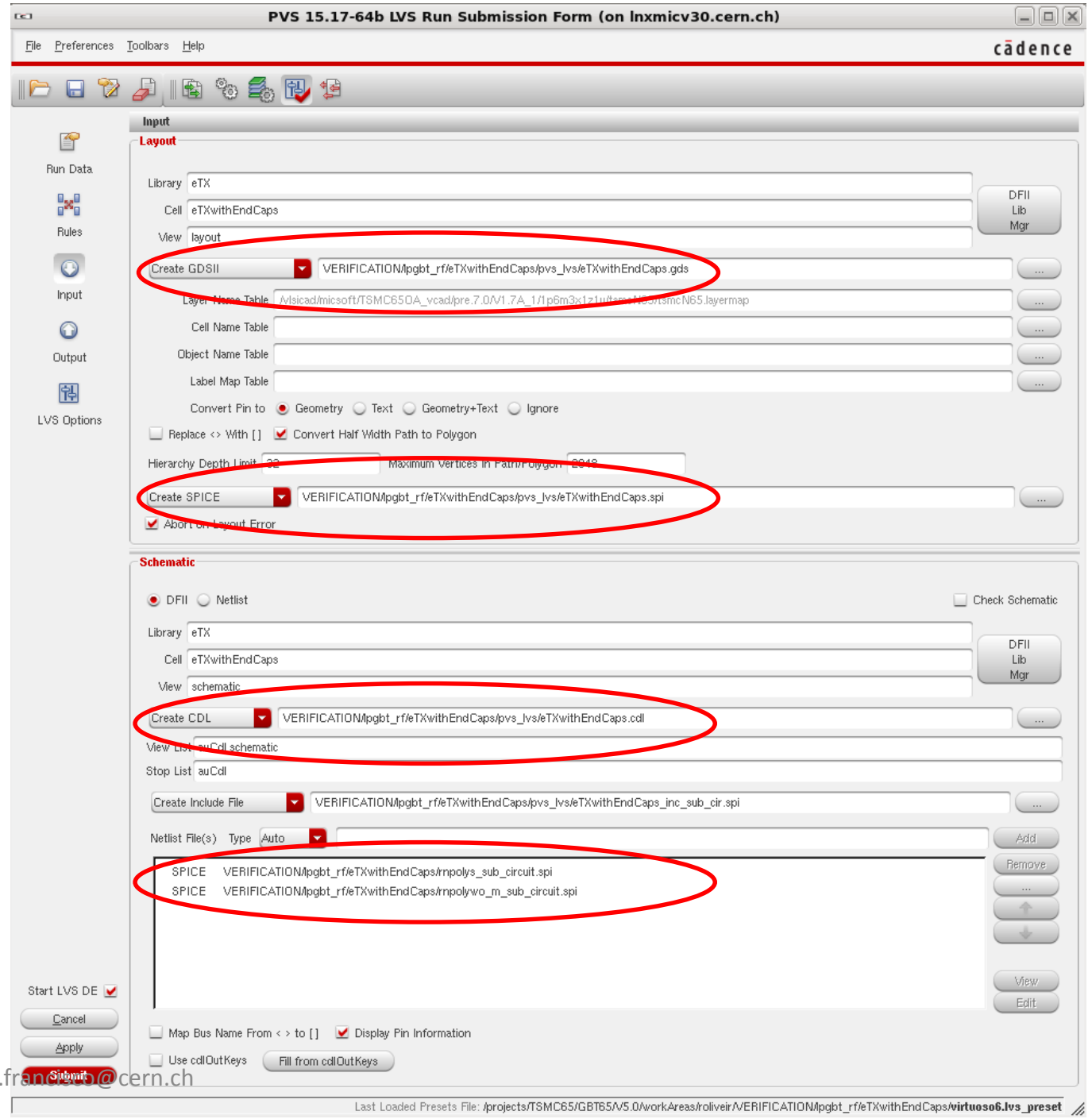
# Run LVS using PVS Setup - Input

- Default options should work to create the GDSII file and the SPICE netlist from layout
- Default options should work to create CDL file
- If needed, include SPICE netlist files





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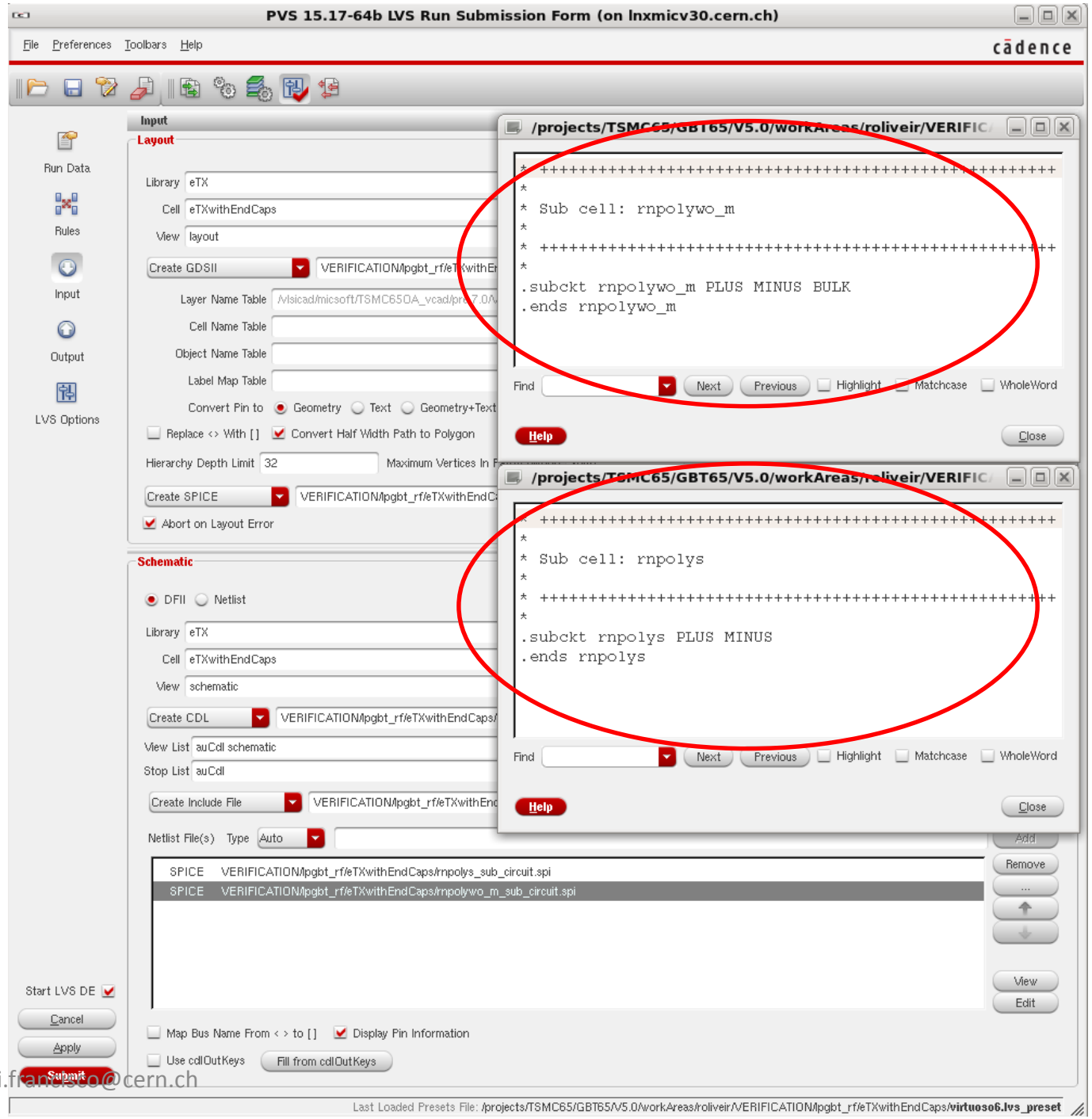
# Run LVS using PVS Setup - SPICE files

- Empty sub-circuit netlist files can be added to filter non existing models



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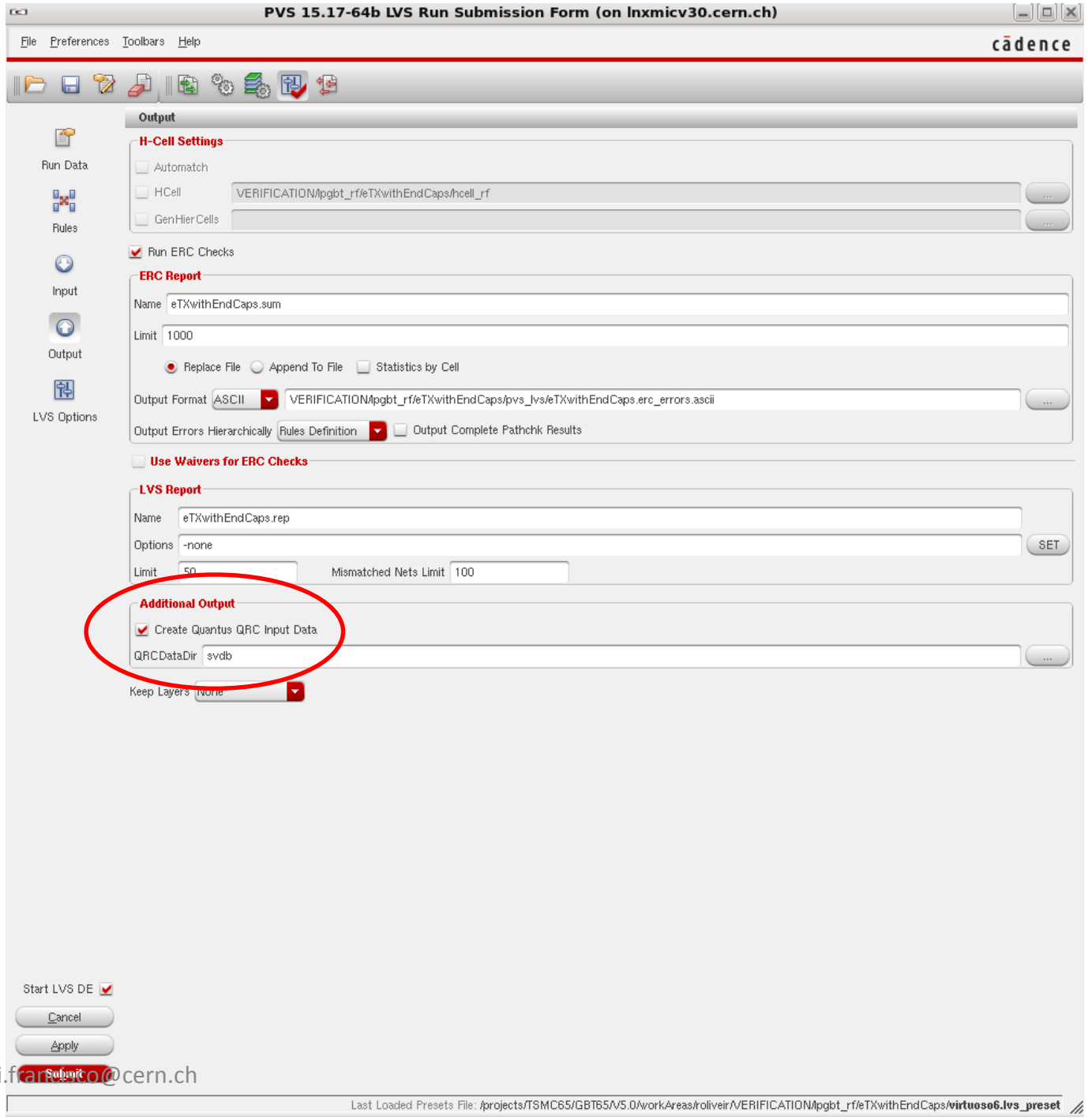
# Run LVS using PVS Setup - Output

- Select “Create Quantus QRC Input Data”
- “svdb” folder will be created inside “Run Directory” already setup in the “Run Data” tab



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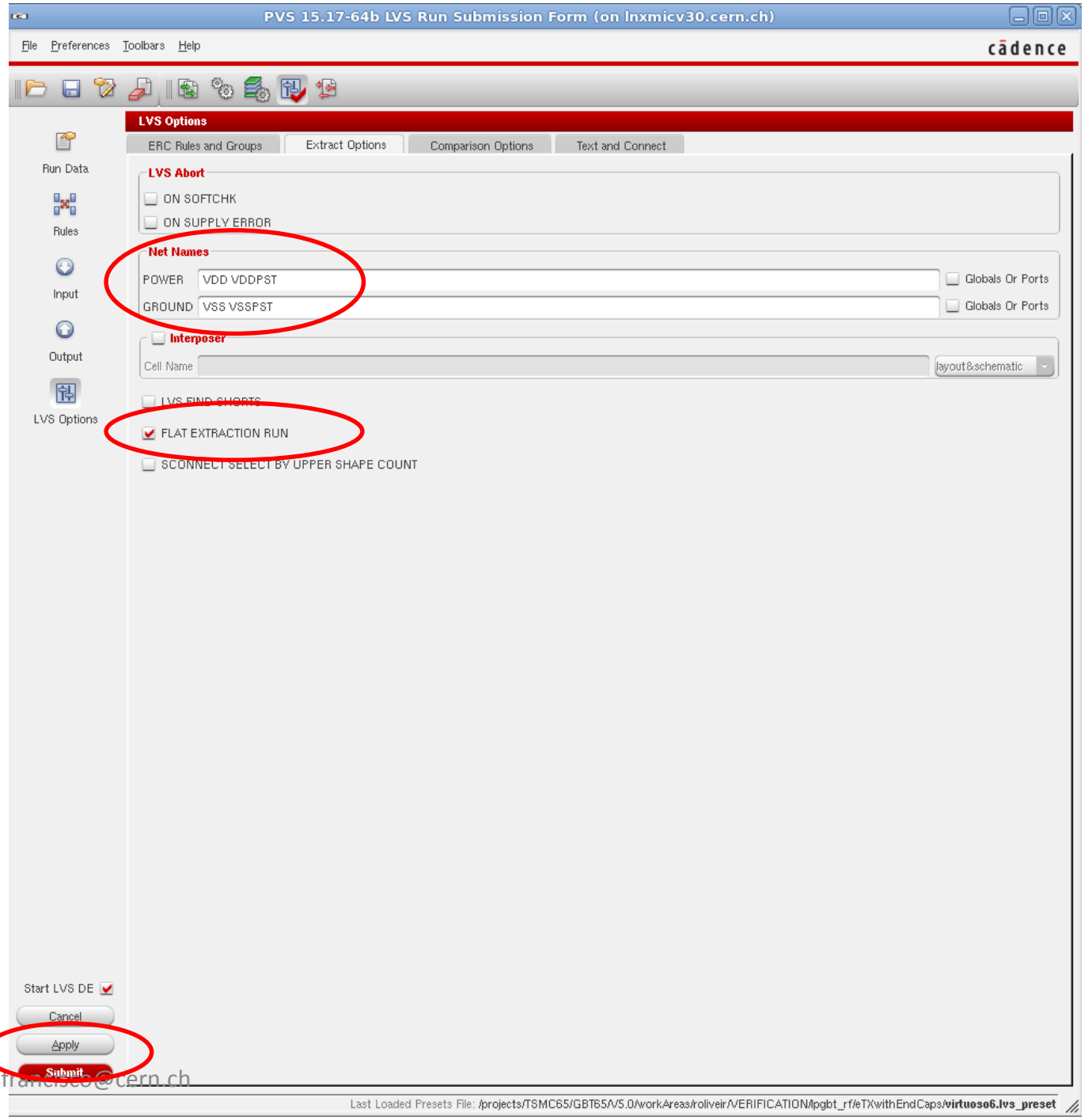
# Run LVS using PVS Setup - LVS Options

- Add Power and Ground net names
- Select Flat Extraction Run

- Click Apply or Submit





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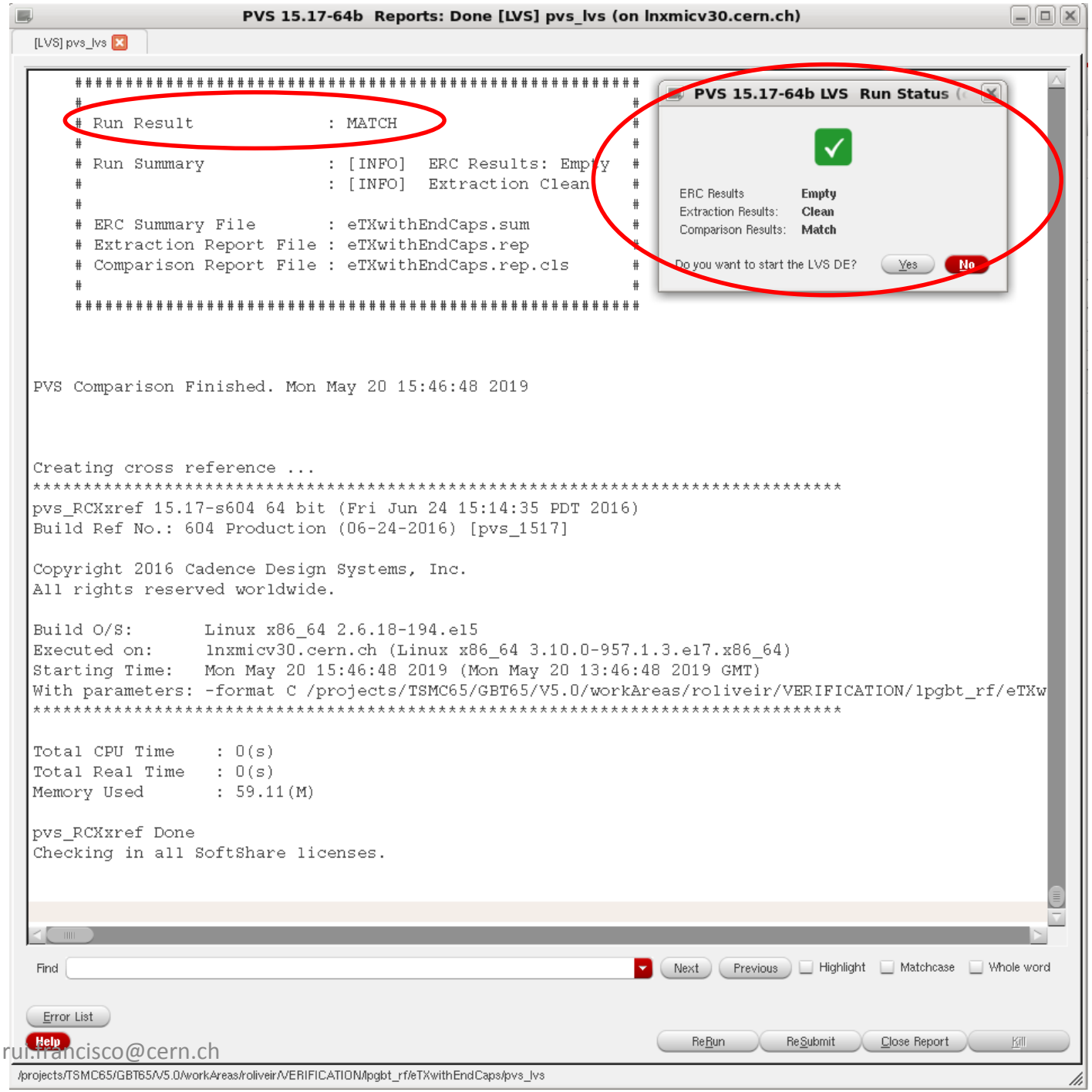
# Run LVS using PVS LVS Results

- LVS should MATCH





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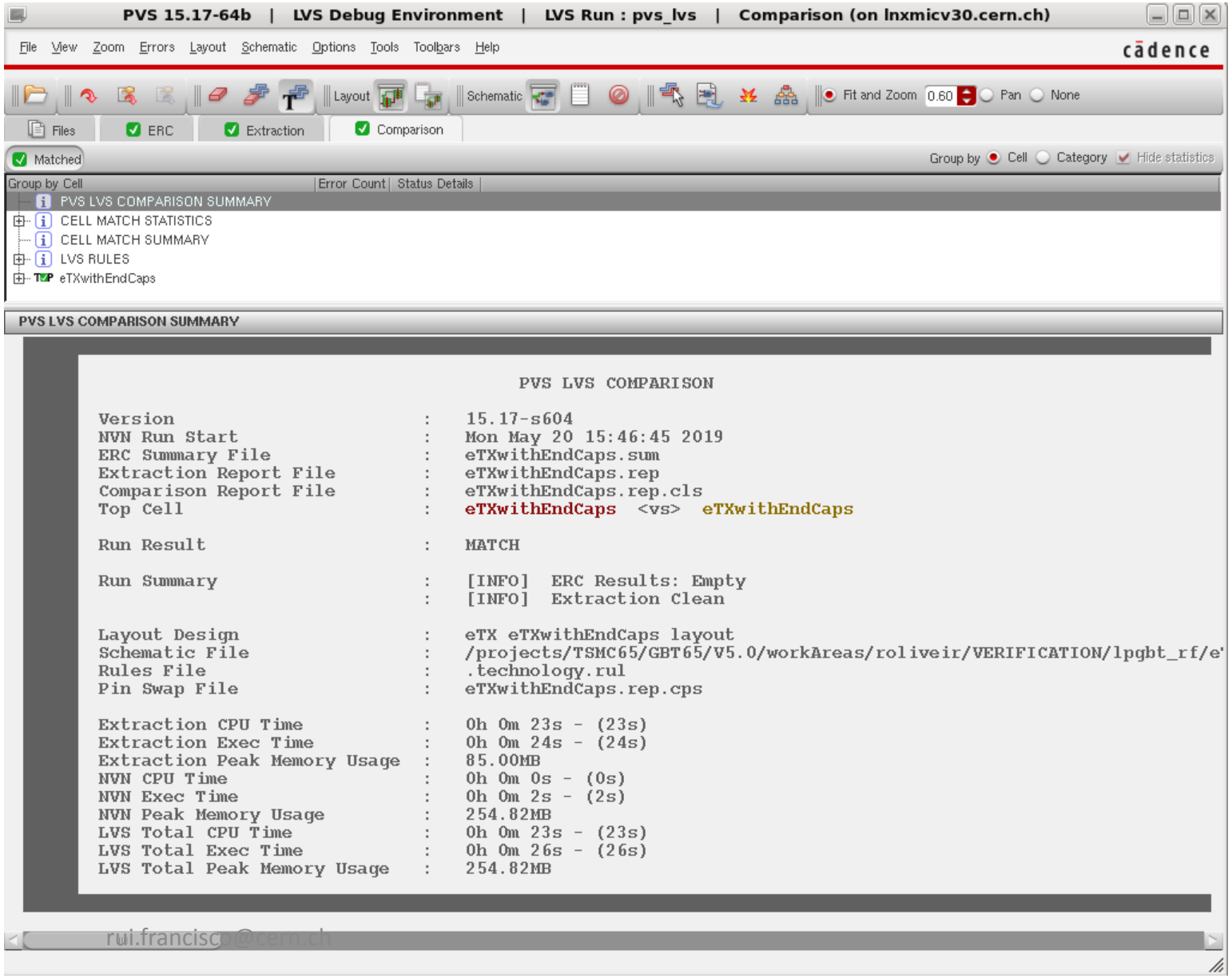
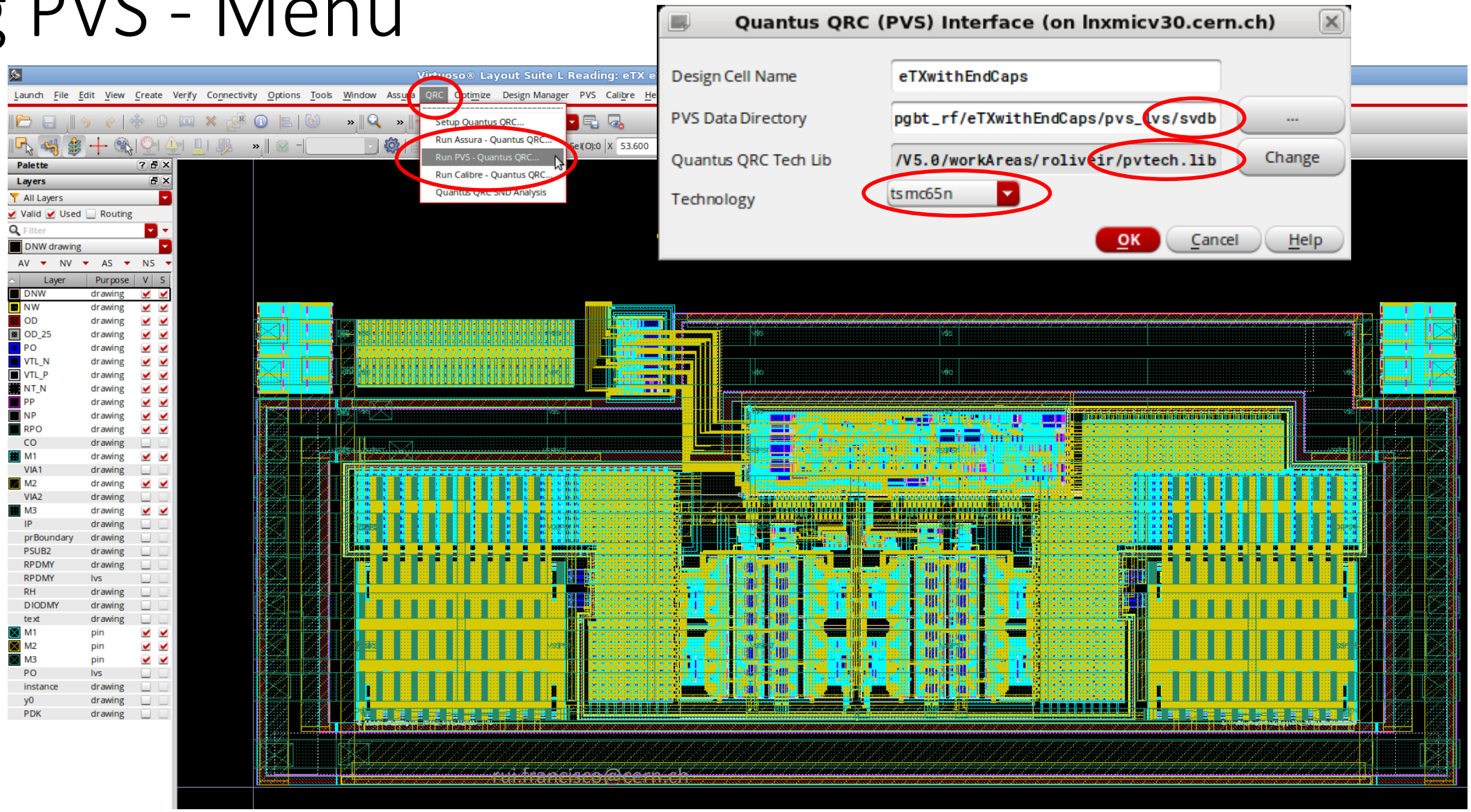
# Run LVS using PVS LVS DE

- If LVS doesn't MATCH, LVS Debug Environment should be used to correct existing issues

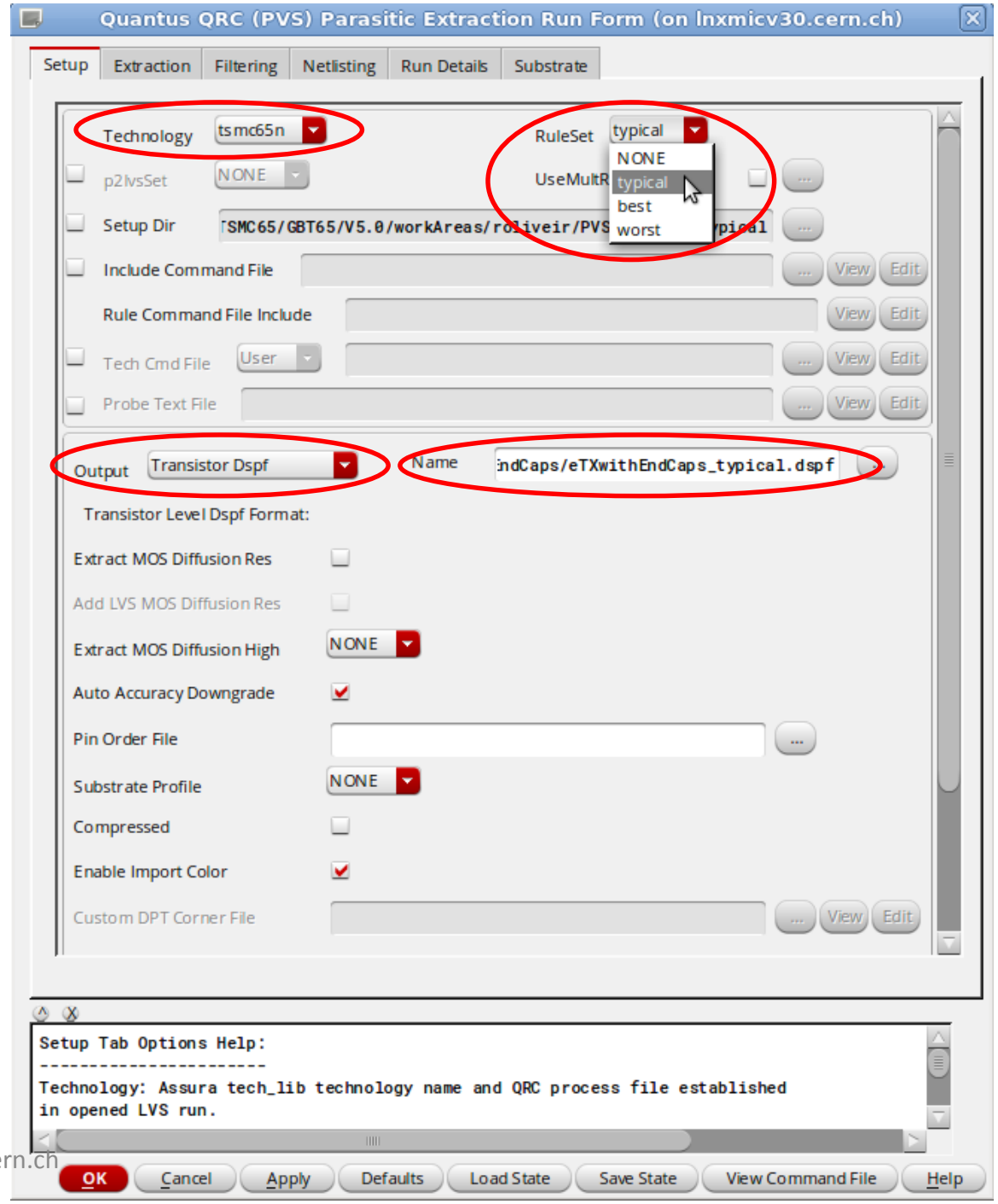


# Run Quantus QRC using PVS - Menu



# Run Quantus QRC using PVS - Setup

- Setup Technology and RuleSet
- Select “Transistor Dspf” for Output type
- Three runs can be executed to create “typical”, “best” and “worst” parasitic RC DSPF files



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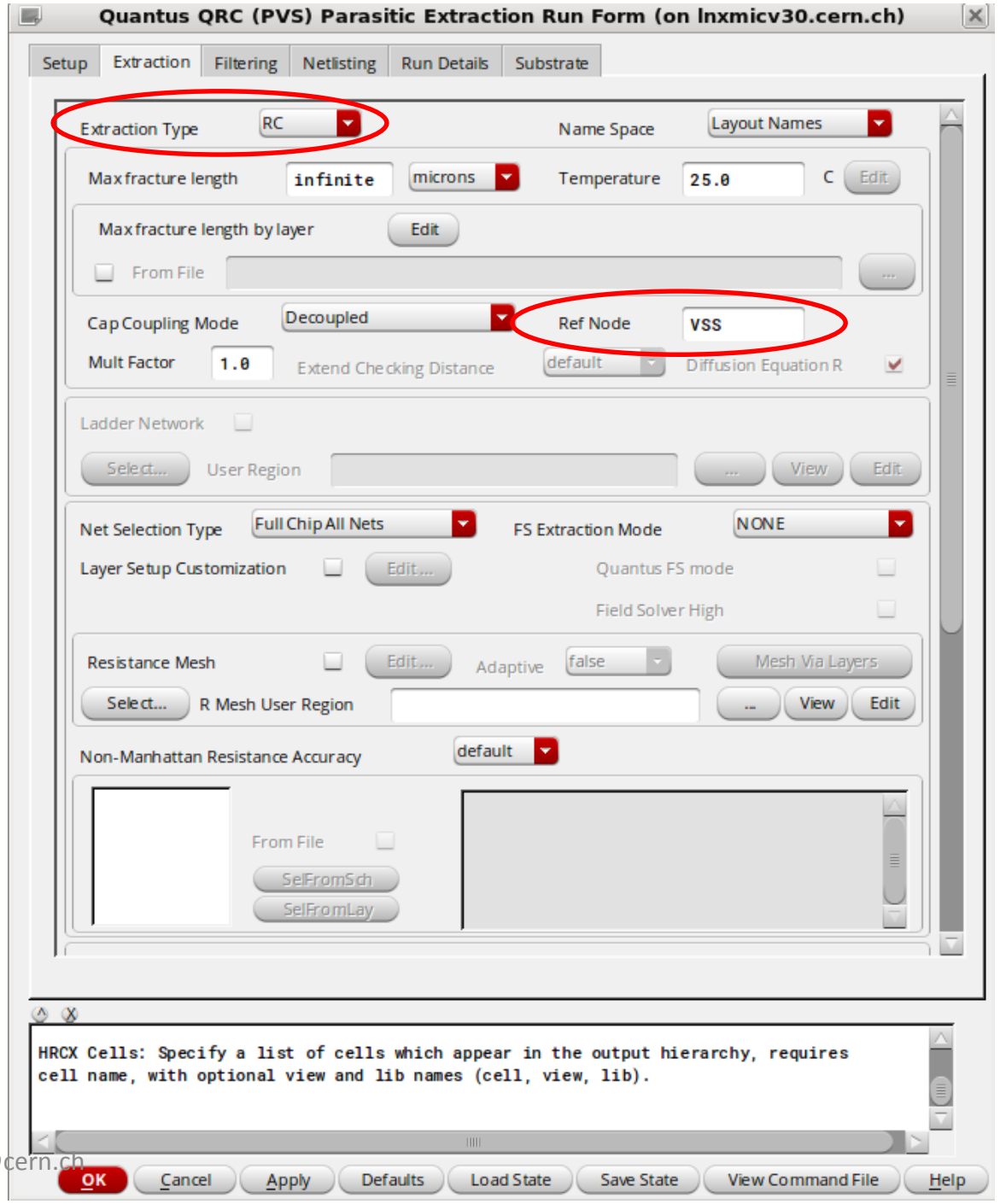
# Run Quantus QRC using PVS - Extraction

- Select RC Extraction Type
- Add Reference Node



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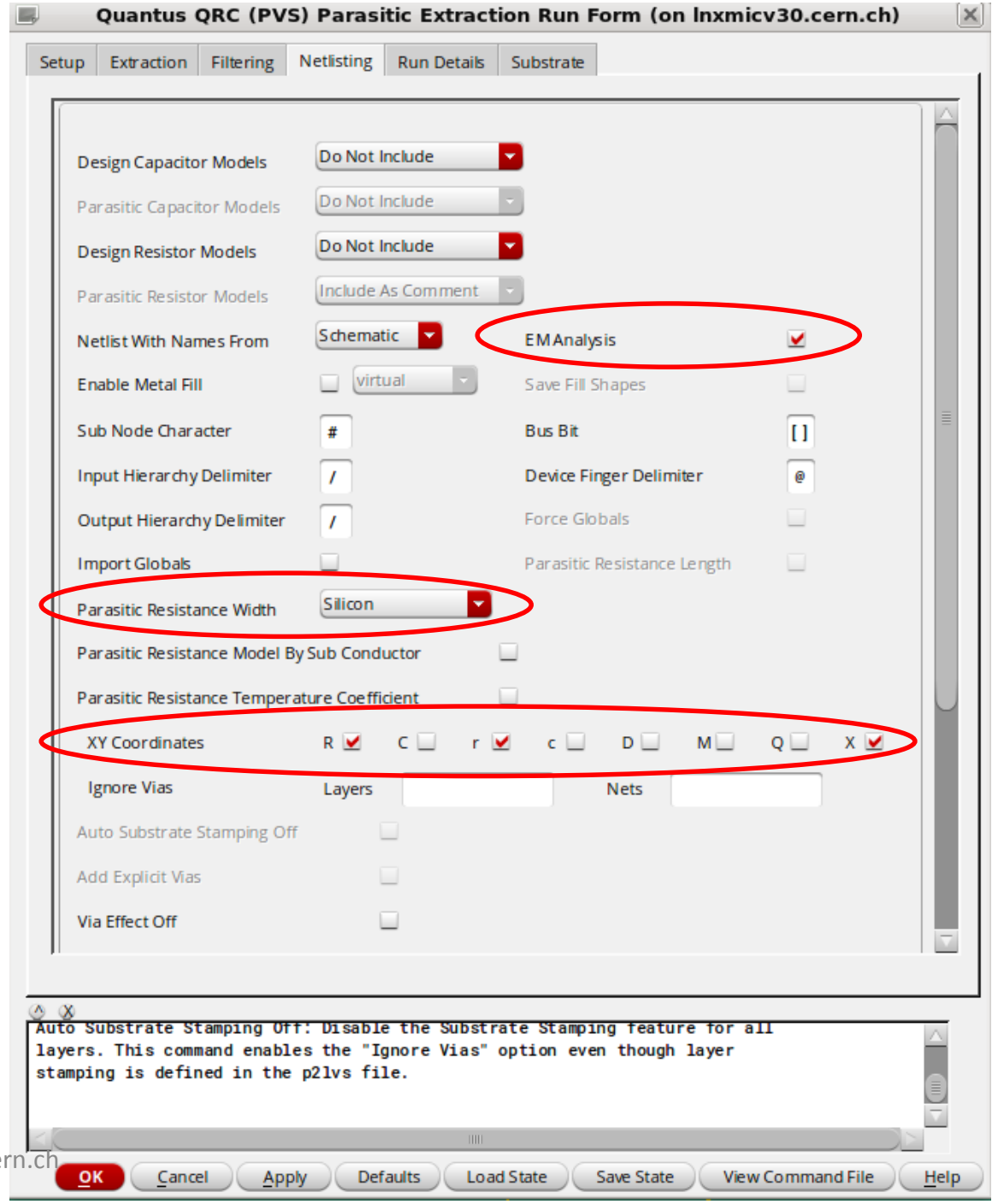
# Run Quantus QRC using PVS - Netlisting

- Select “EM Analysis”

- Select “Silicon” for “Parasitic Resistance Width”
- Select XY Coordinates for the parasitics



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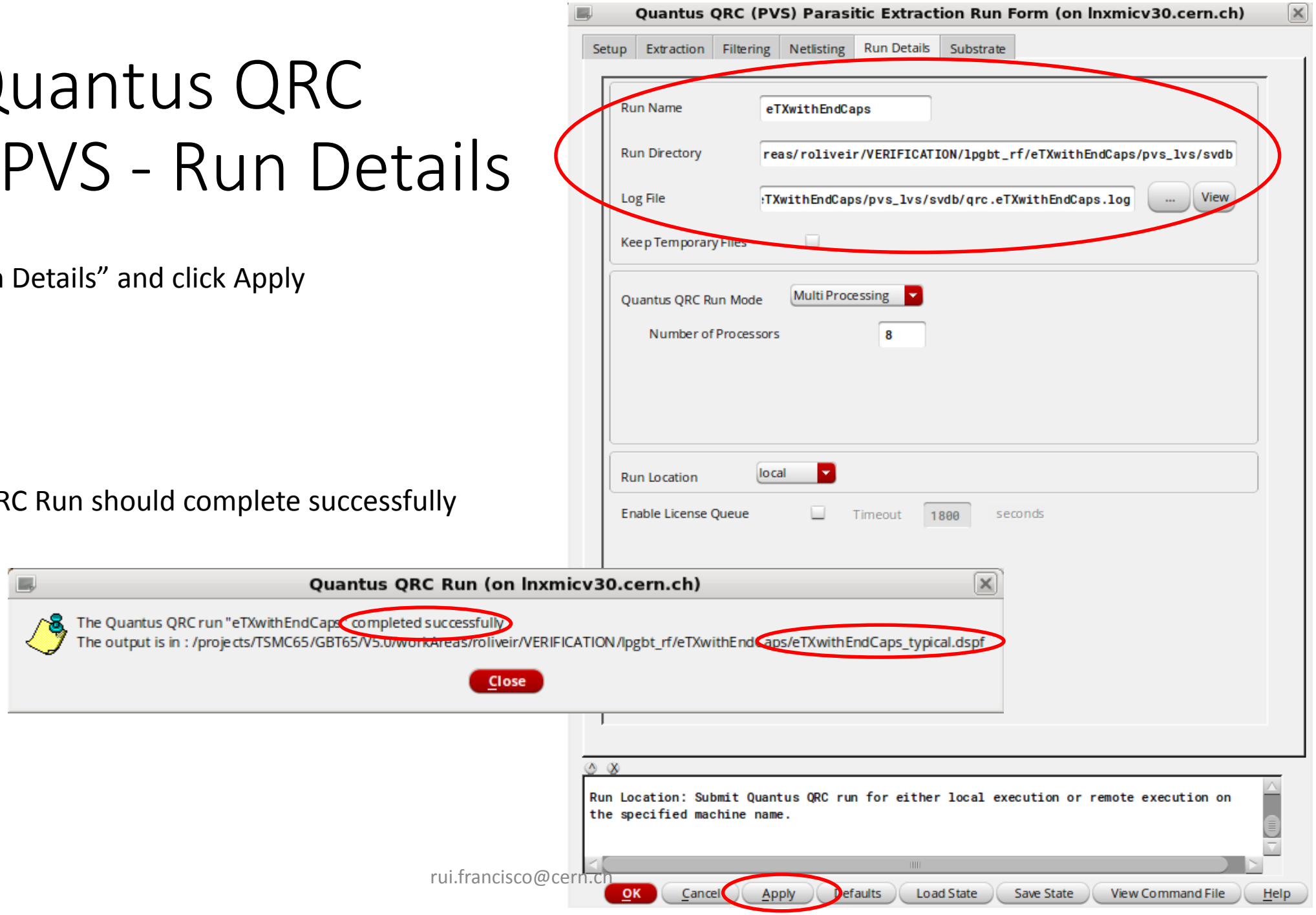
# Run Quantus QRC using PVS - Run Details

- Check “Run Details” and click Apply

- Quantus QRC Run should complete successfully



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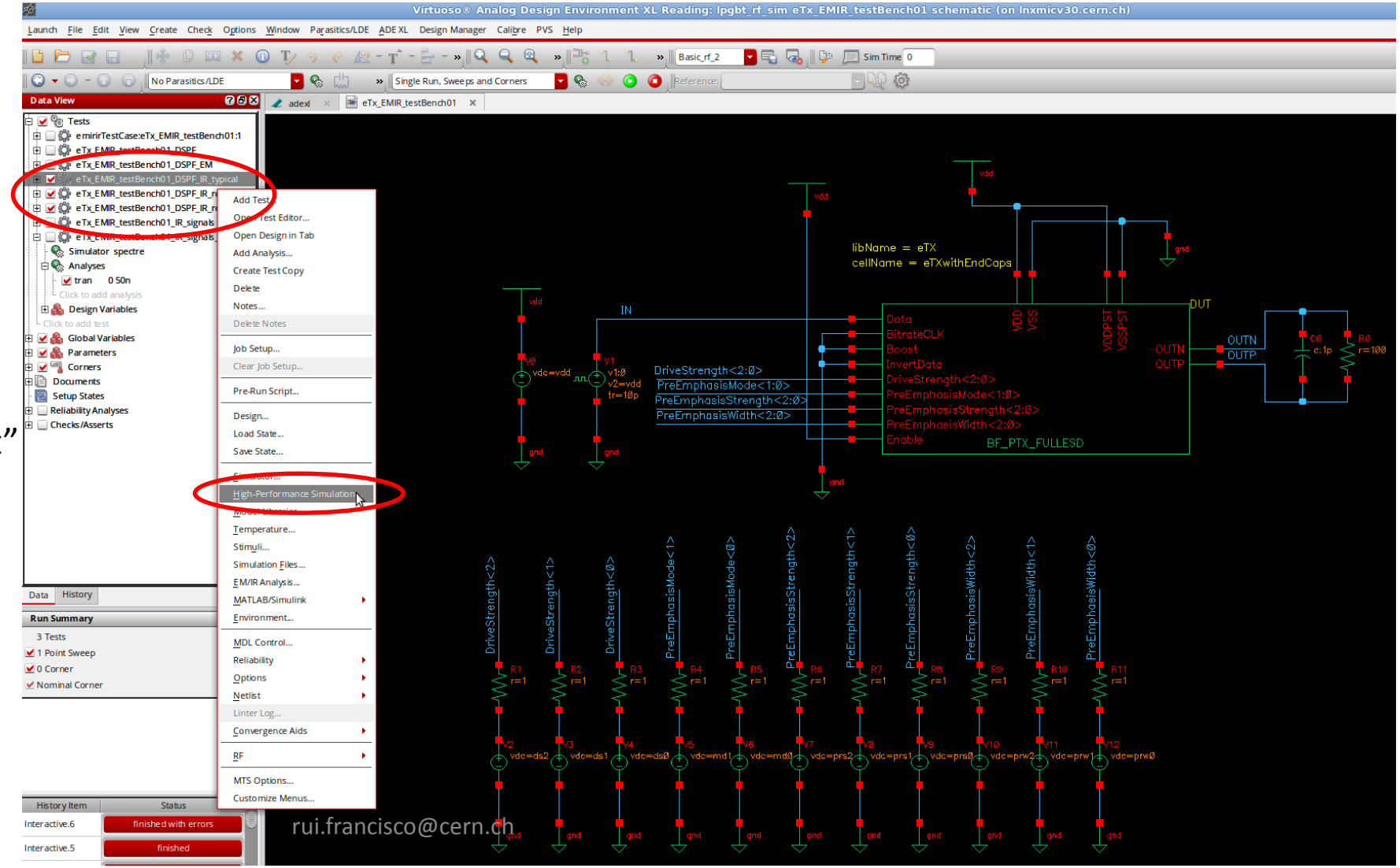
# Run Simulation ADEXL
# High Performance Simulation

- Open the previously used ADEXL view
- Select the previously used Test or create new ones
- Three test cases can be created for “typical”, “best” and “worst” DSPF files
- RMB test name and select “High-Performance Simulation”



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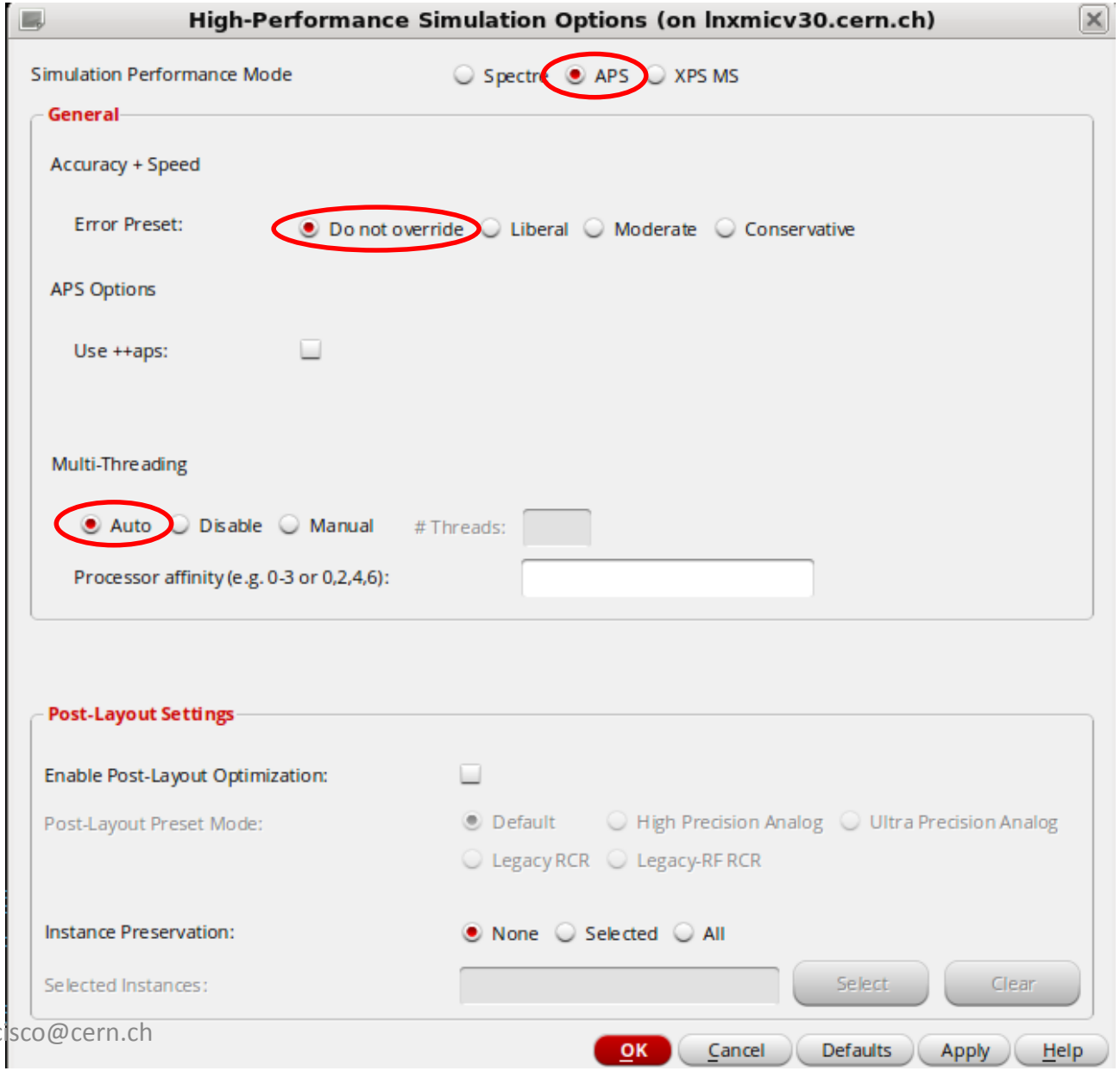
# Run Simulation ADEXL APS Options

- Select “APS”, “Do not override” and “Auto”



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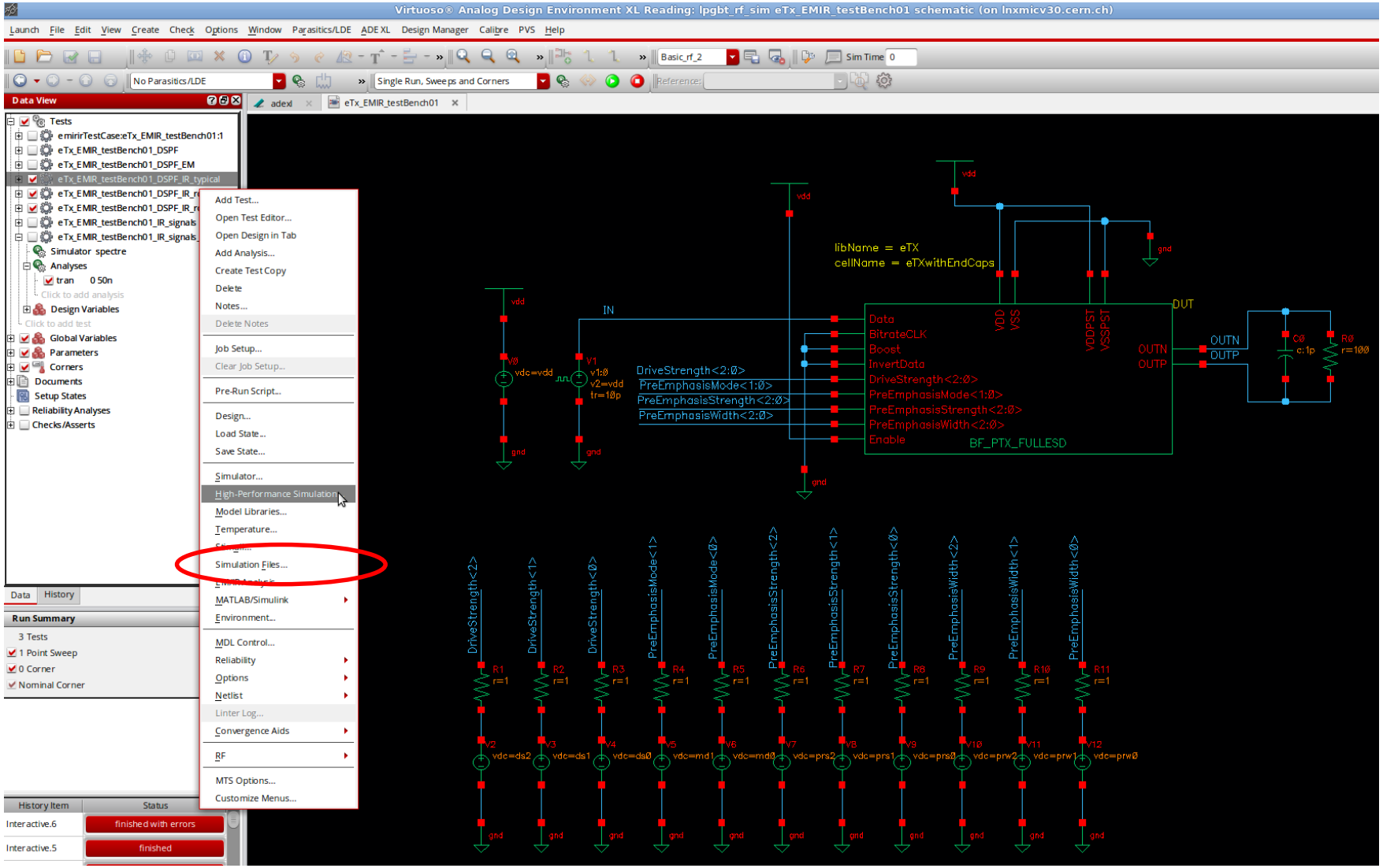
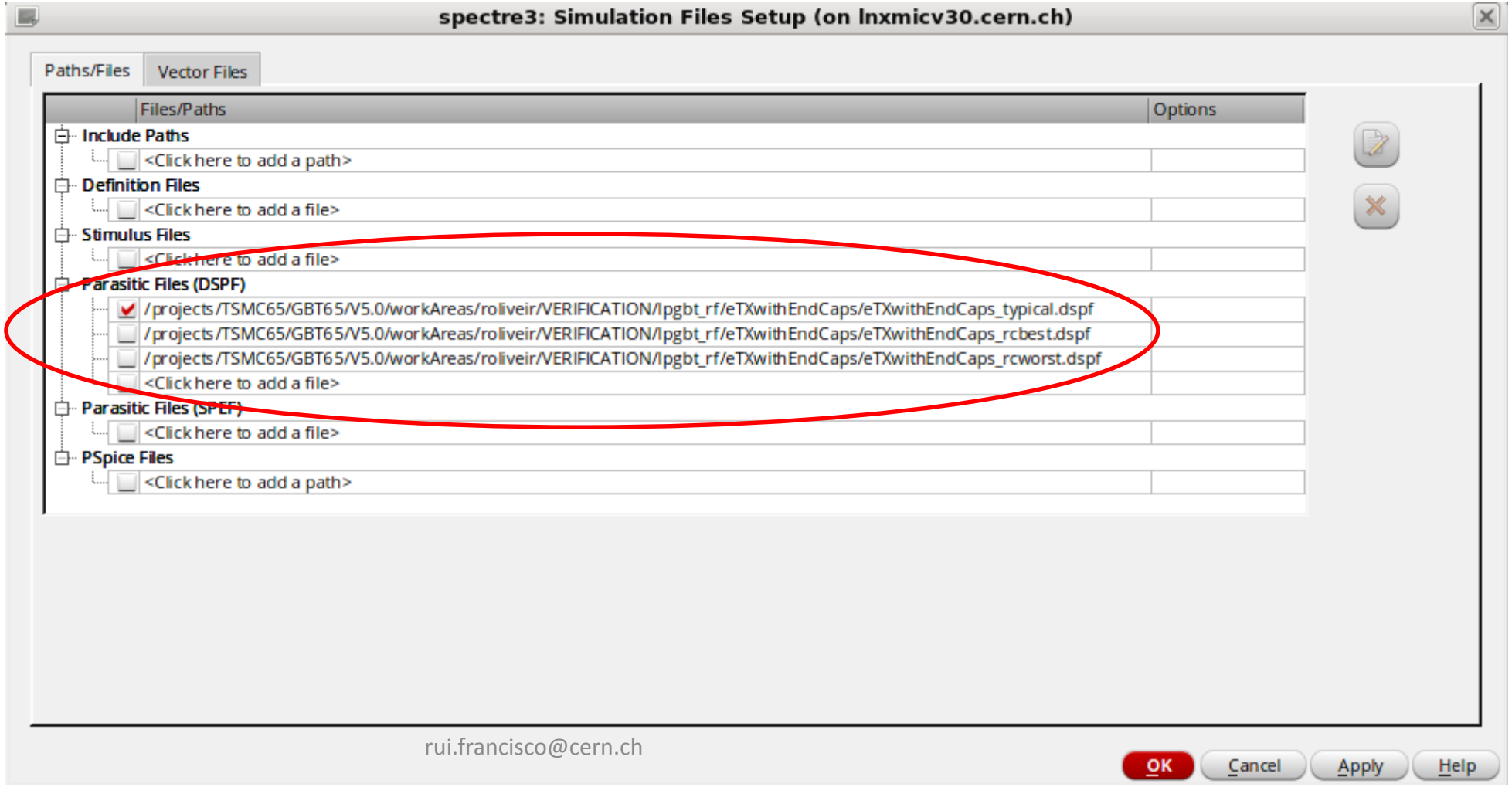
# Run Simulation ADEXL Simulation Files - DSPF

- RMB test name and select “Simulation Files”



# Run Simulation ADEXL Simulation Files - DSPF

- Add DSPF files to “Parasitic Files”
- Select DSPF file according to test case





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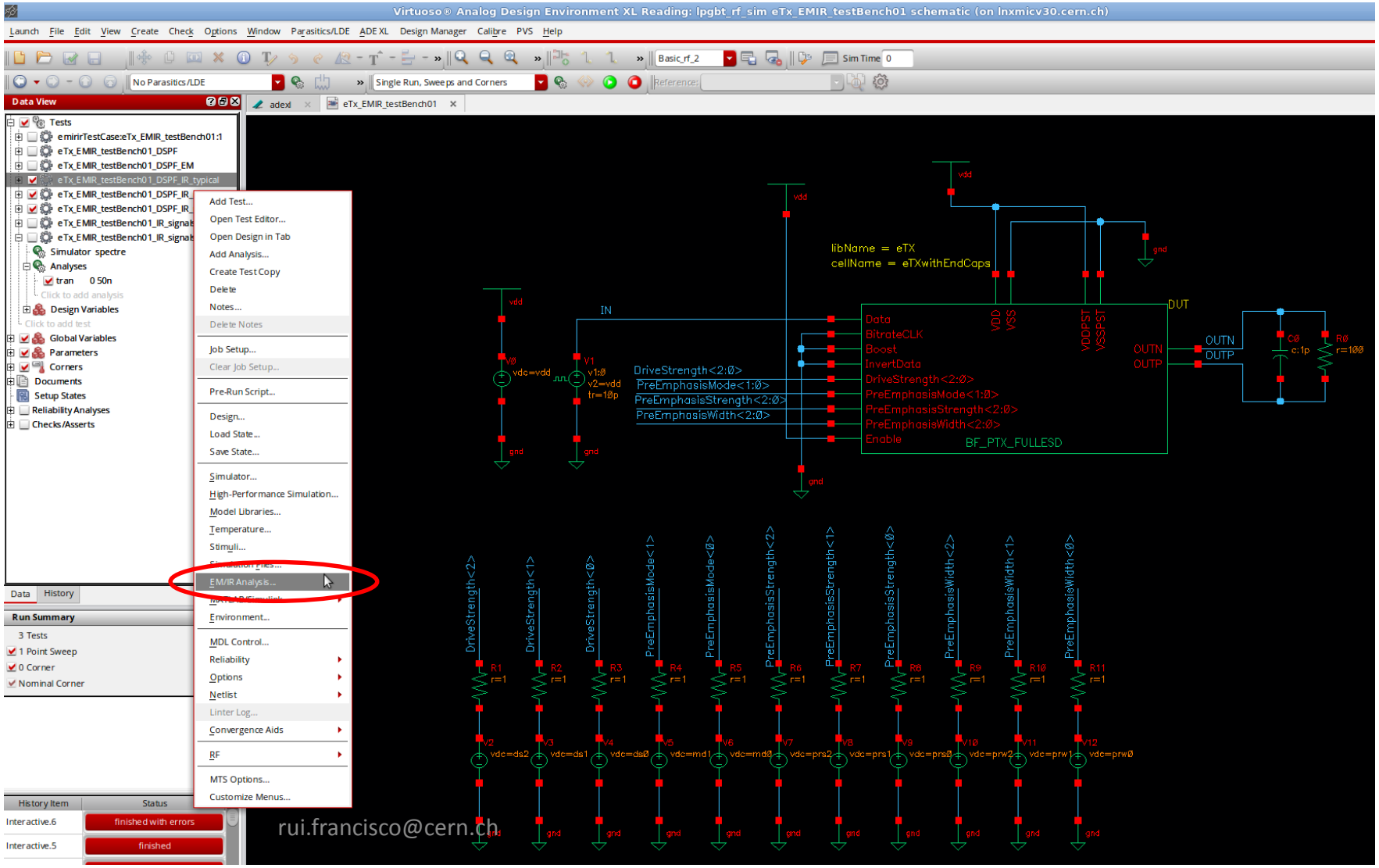
# Run Simulation ADEXL EM/IR Analysis

- RMB test name and select “EM/IR Analysis”



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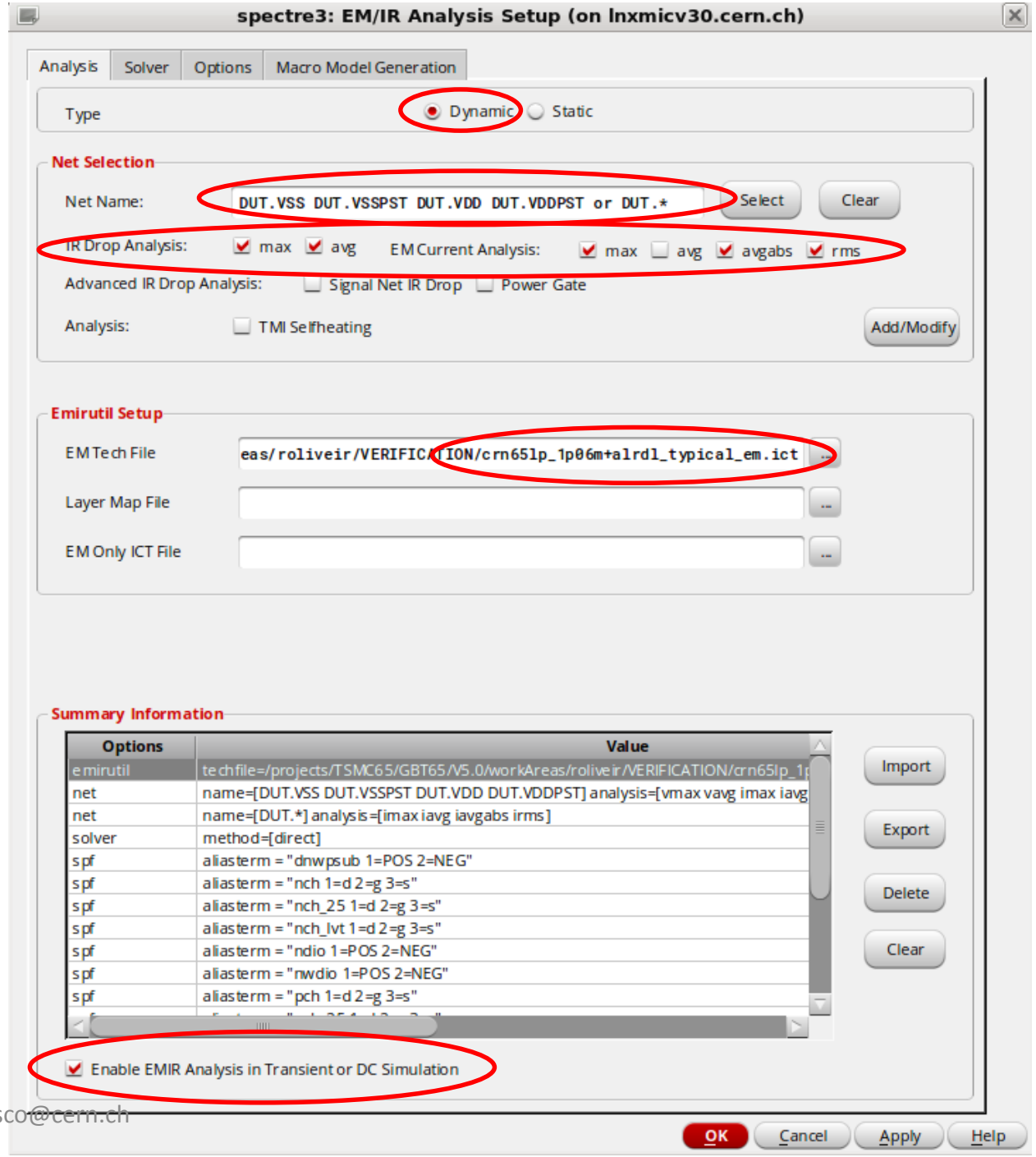
# Run Simulation ADEXL Setup - Analysis

- Select Type of Analysis
- Select Nets
- Select Type of Analysis for the Nets
- Default configuration allows:
  - IR Power Analysis
  - EM Power and Signals Analysis

- Browse for and Select the adequate “*_em.ict” file

- Select “Enable EMIR Analysis in Transient or DC Simulation”





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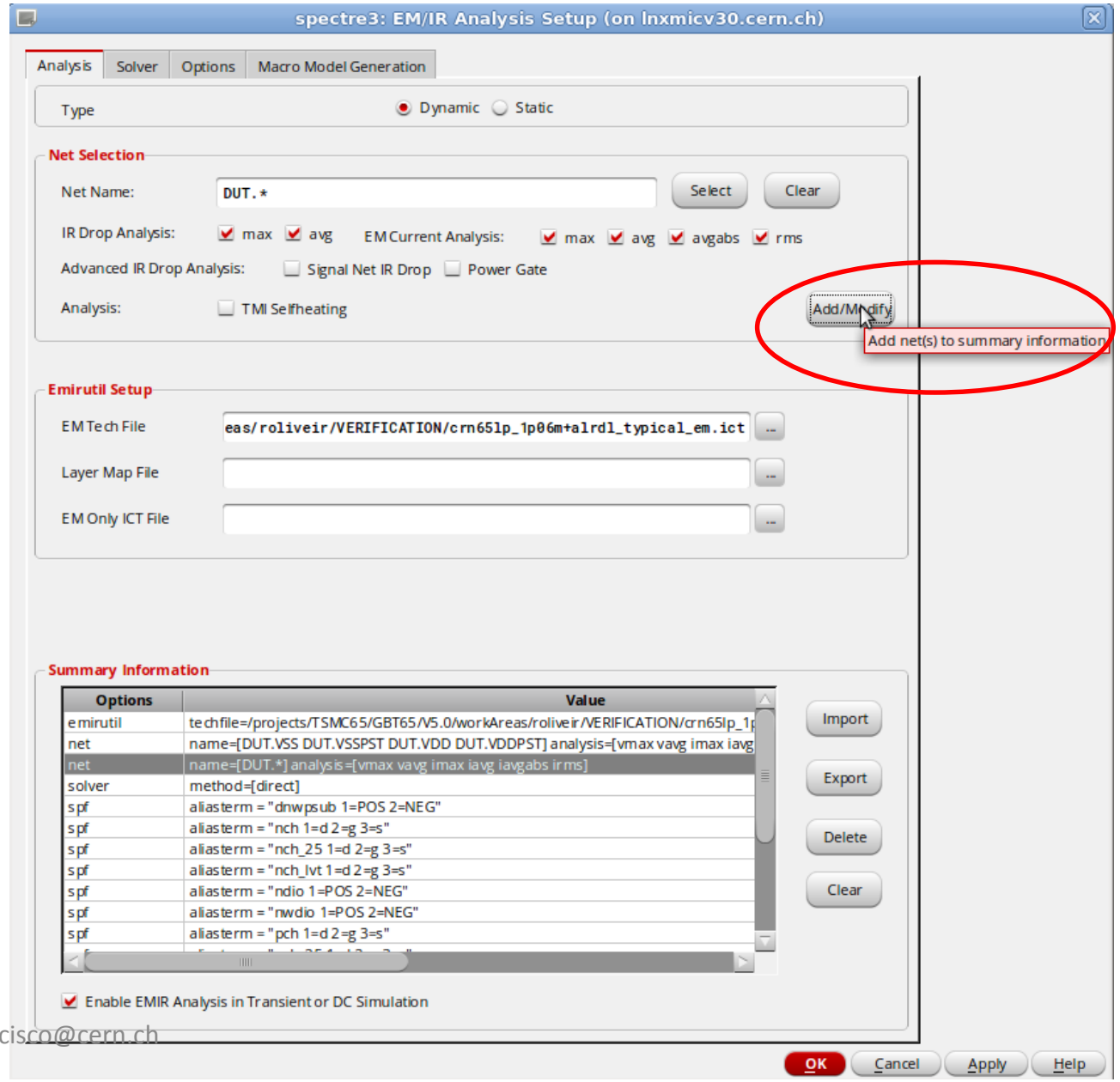
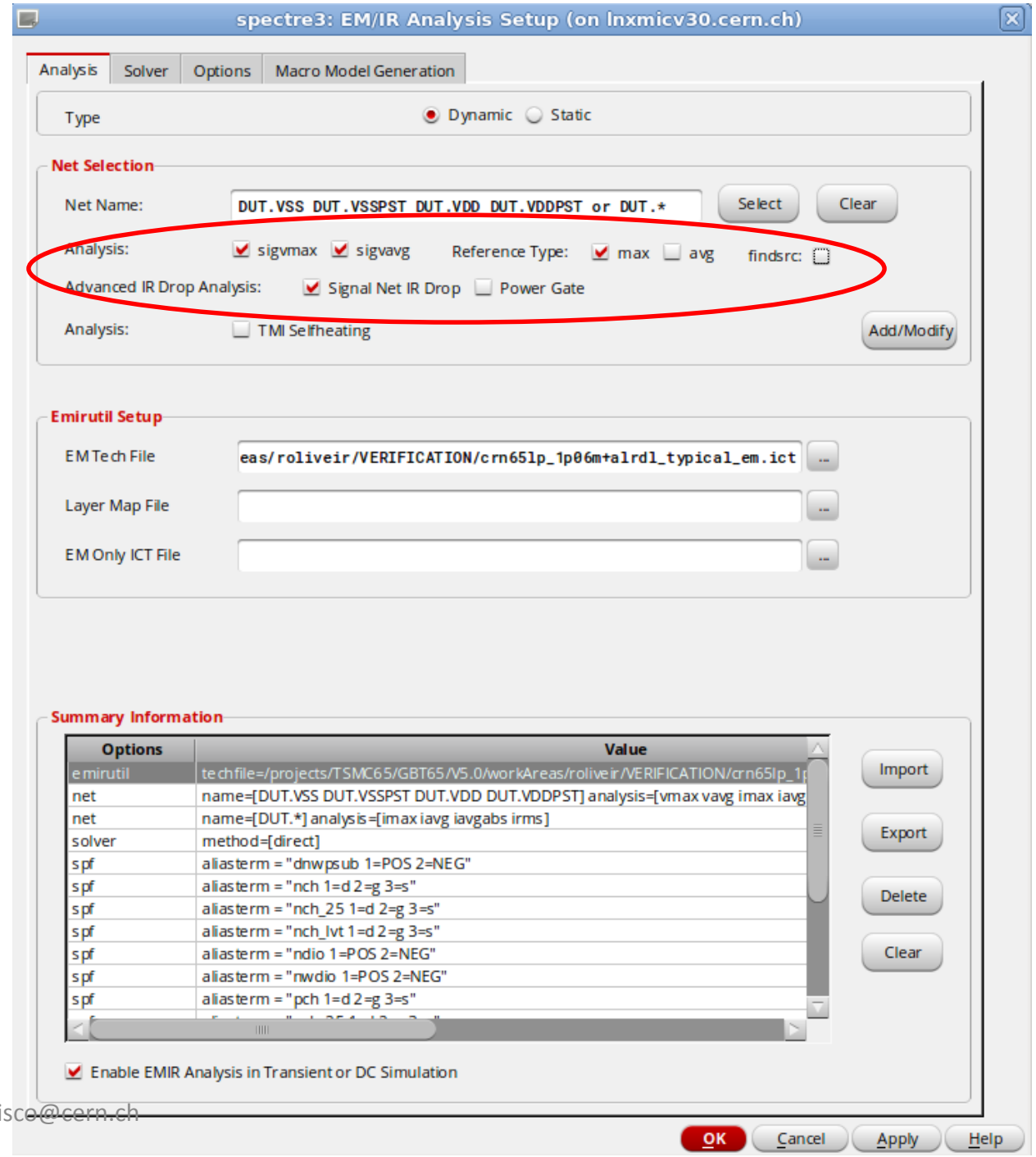
# Run Simulation ADEXL Setup - Analysis

- Click Add/Modify if changes were done



# Run Simulation ADEXL Setup - Analysis

- For IR Signals Analysis select Advanced IR Drop Analysis: Signal Net IR Drop





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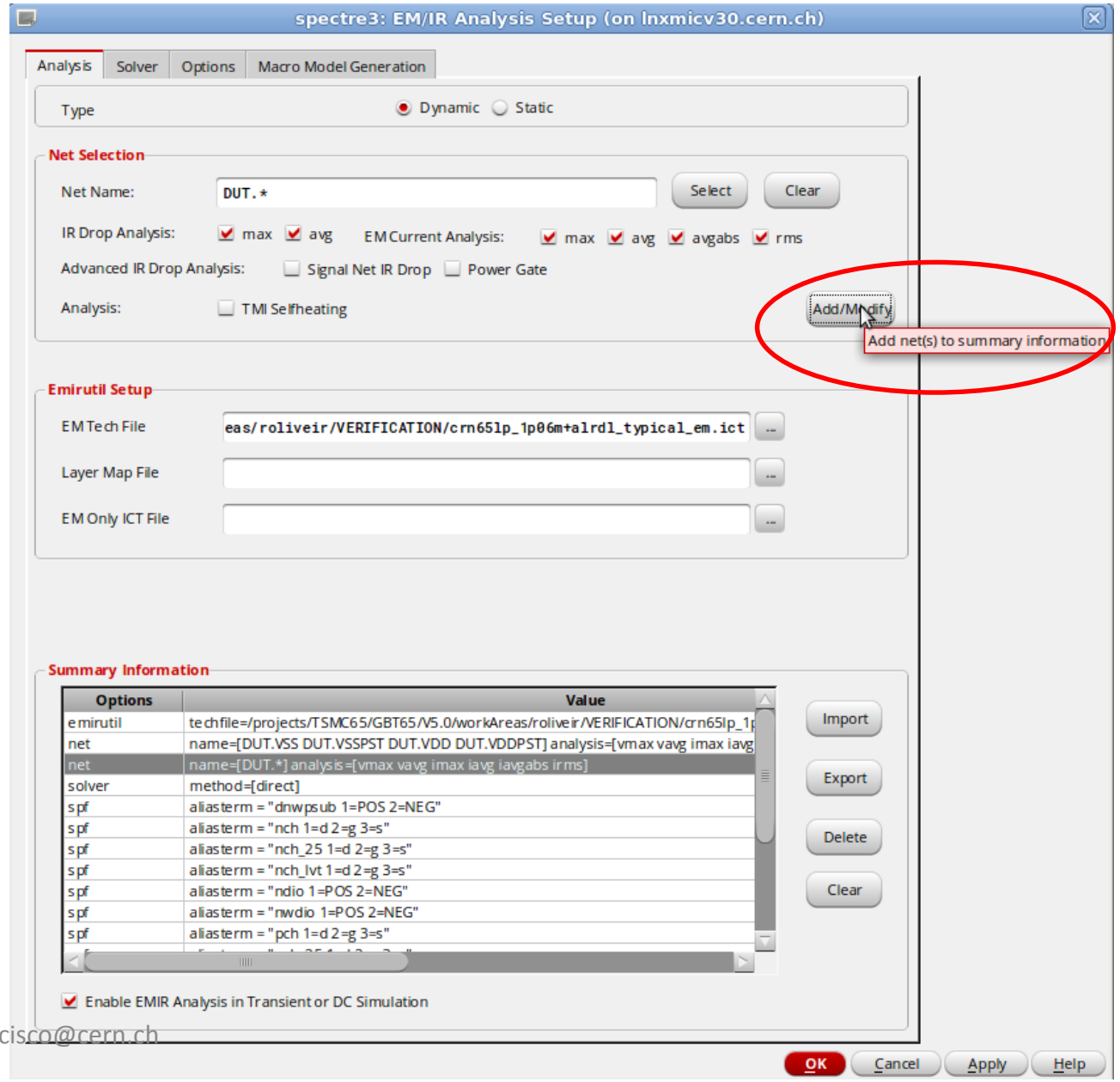
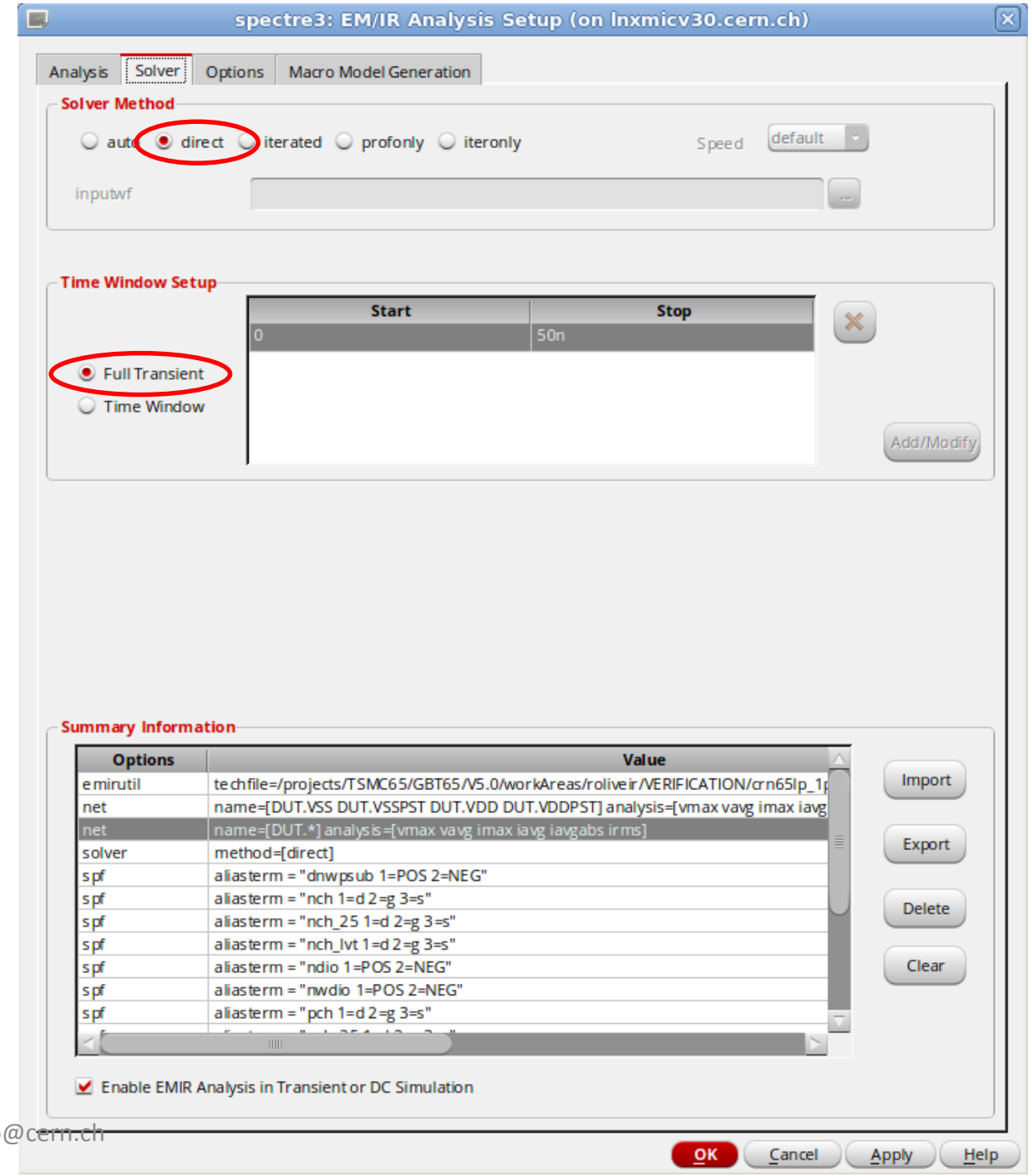
# Run Simulation ADEXL Setup - Analysis

- Click Add/Modify if changes were done



# Run Simulation ADEXL Setup - Solver

- Select “direct” for Solver Method
- Choose the Time Window



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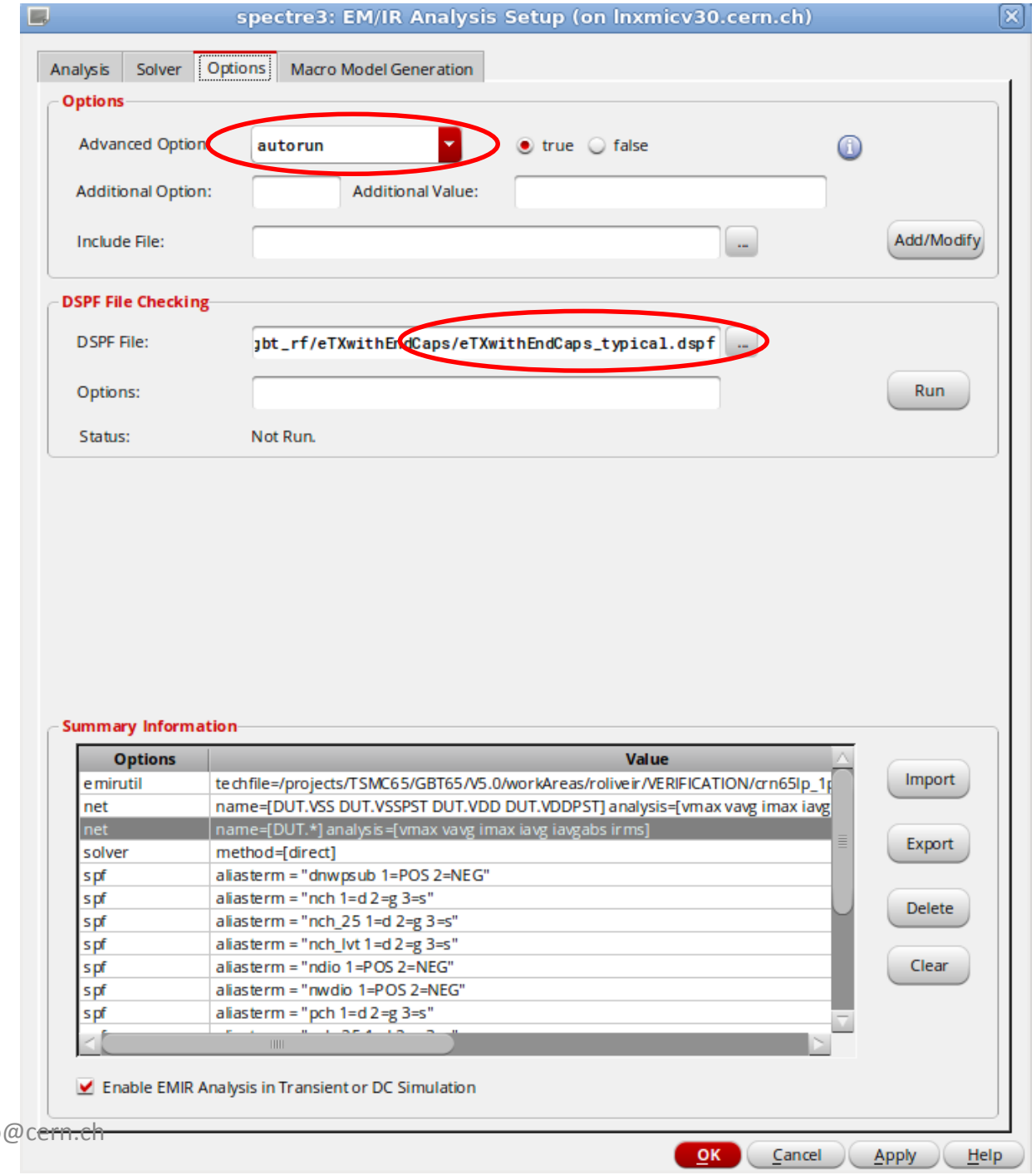
# Run Simulation ADEXL Setup - Options

- Select “autorun”
- Add the adequate DSPF file, the same previously chosen in Simulation Files





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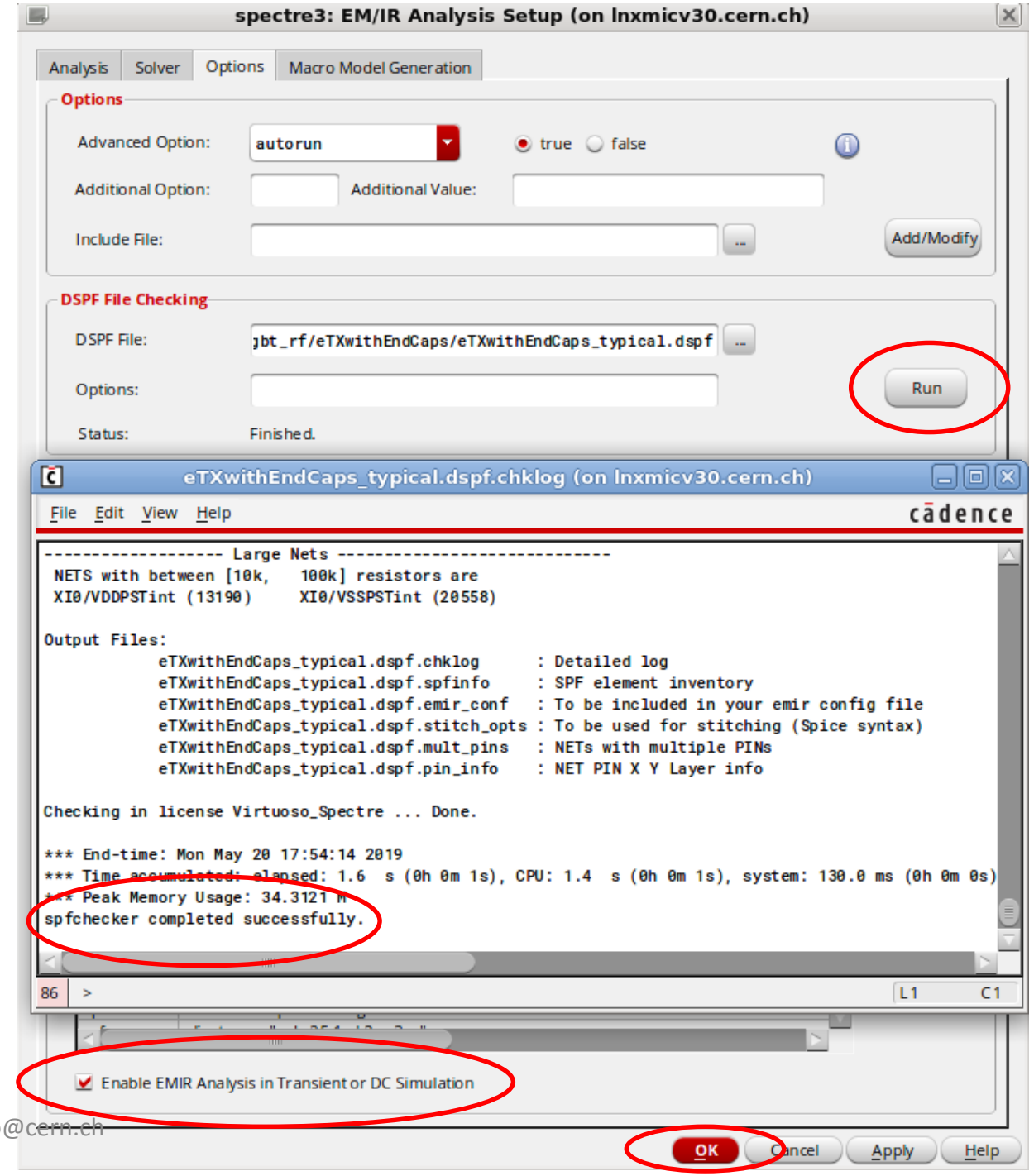
# Run Simulation ADEXL Setup - DSPF Checker

- Run the DSPF checker
- The checker should complete successfully
- Click “OK” after verifying that “Enable EMIR Analysis in Transient or DC Simulation” is ENABLED





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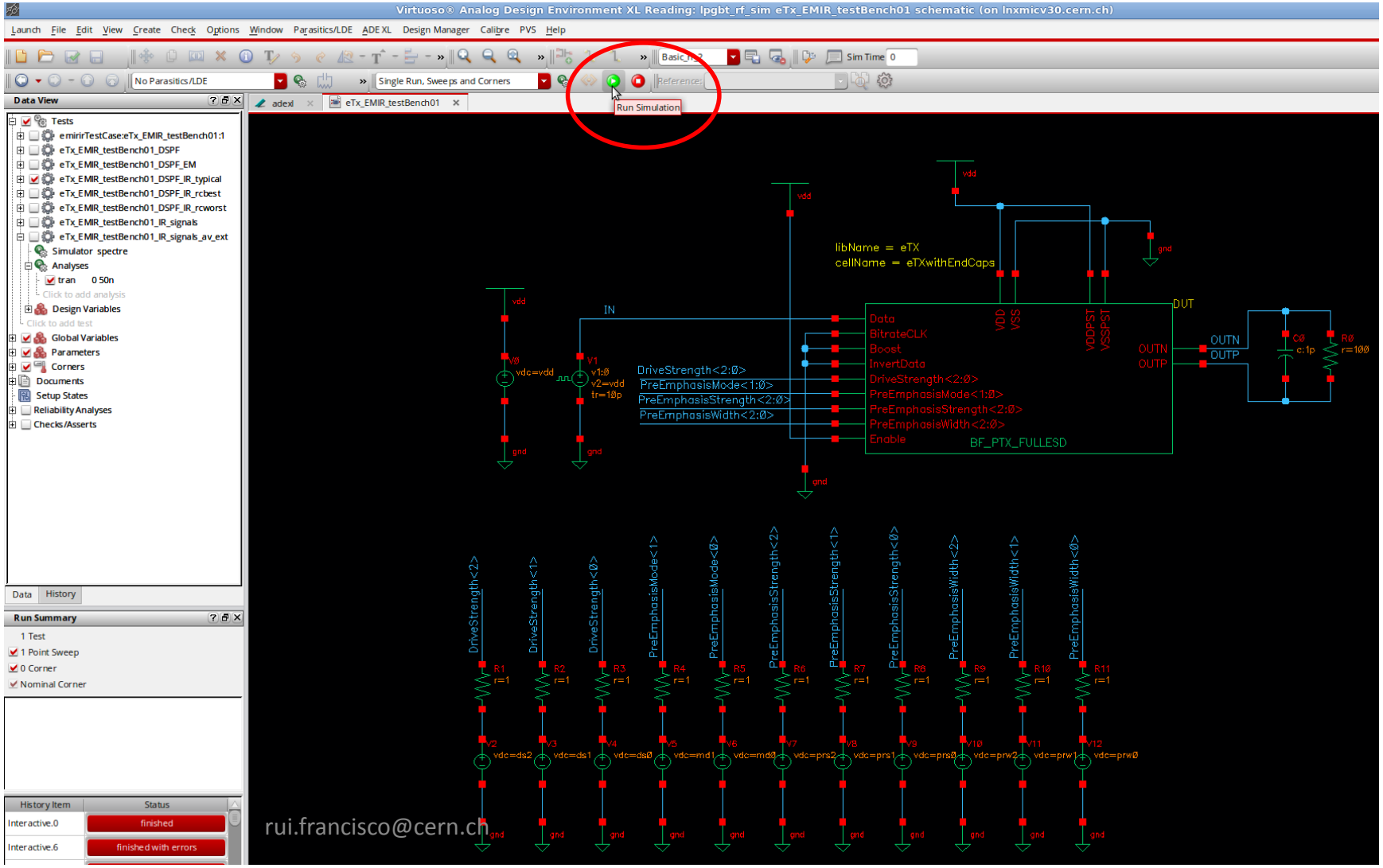
# Run Simulation ADEXL
# Run Simulation

- Run the Simulation



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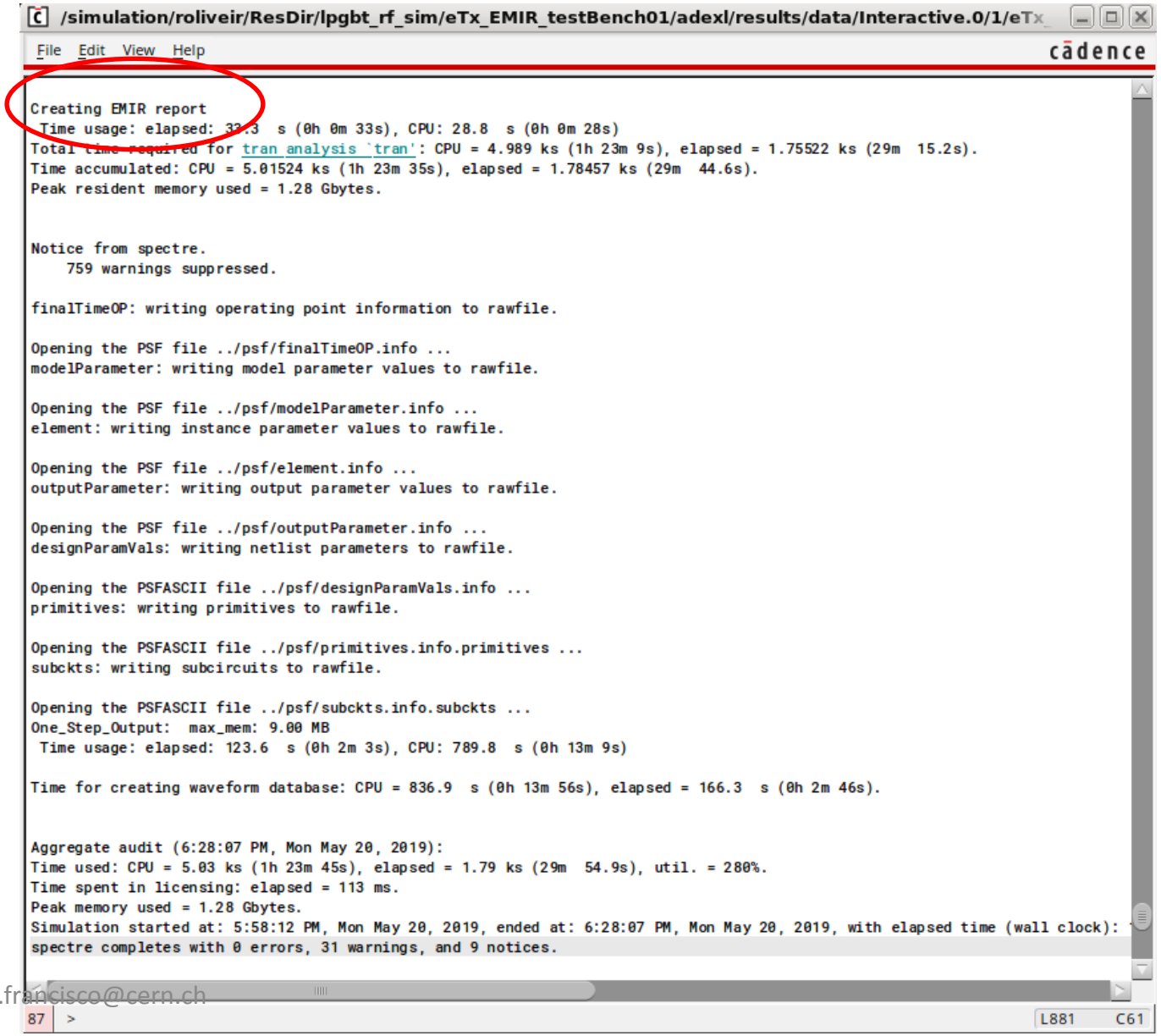
# Run Simulation ADEXL EMIR Report

- Simulation log should show “Creating EMIR report”





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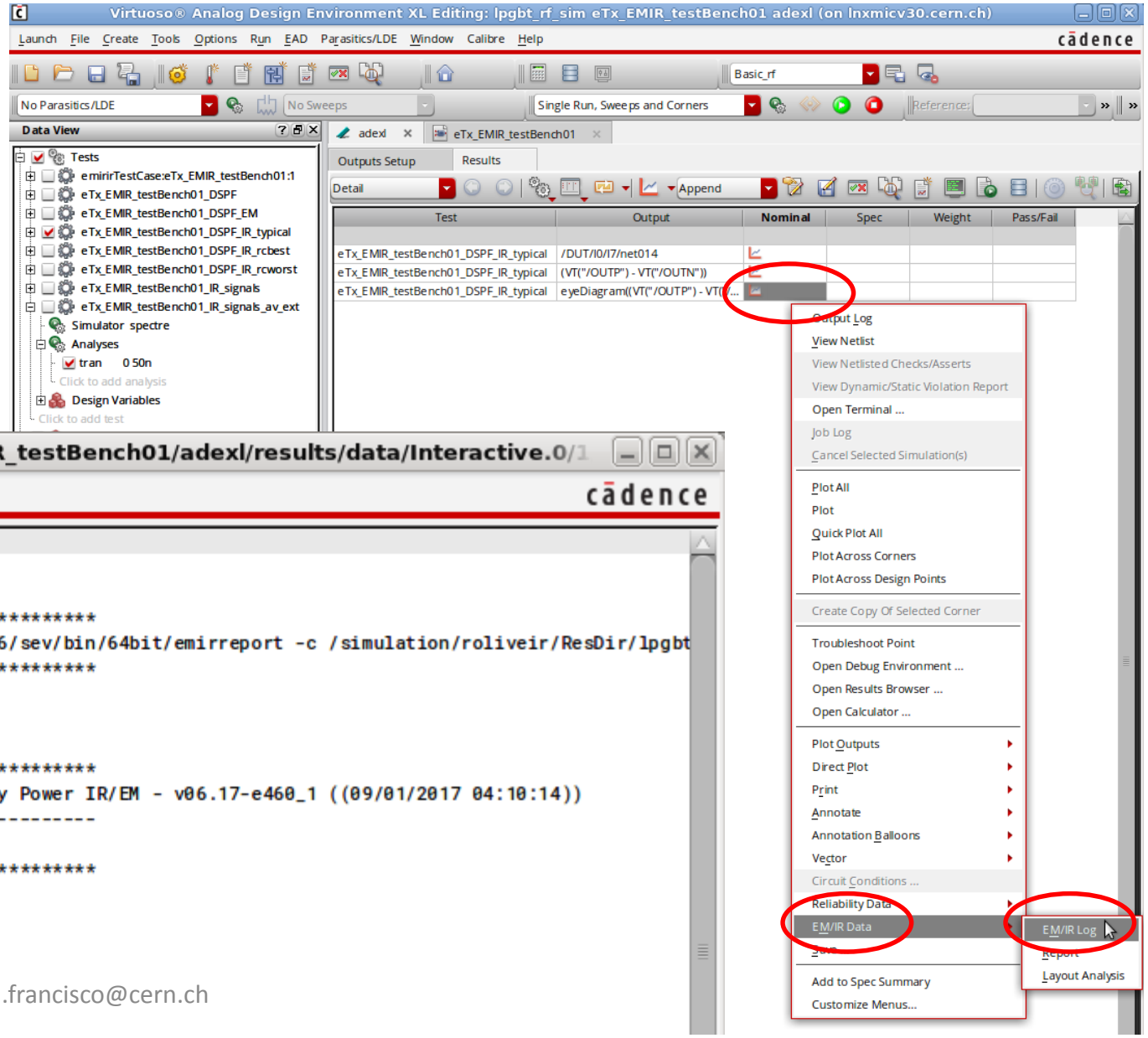
# Run Simulation ADEXL EMIR Log

- EMIR Analysis log can be checked with RMB over results in the Results tab, EM/IR Data, EM/IR Log





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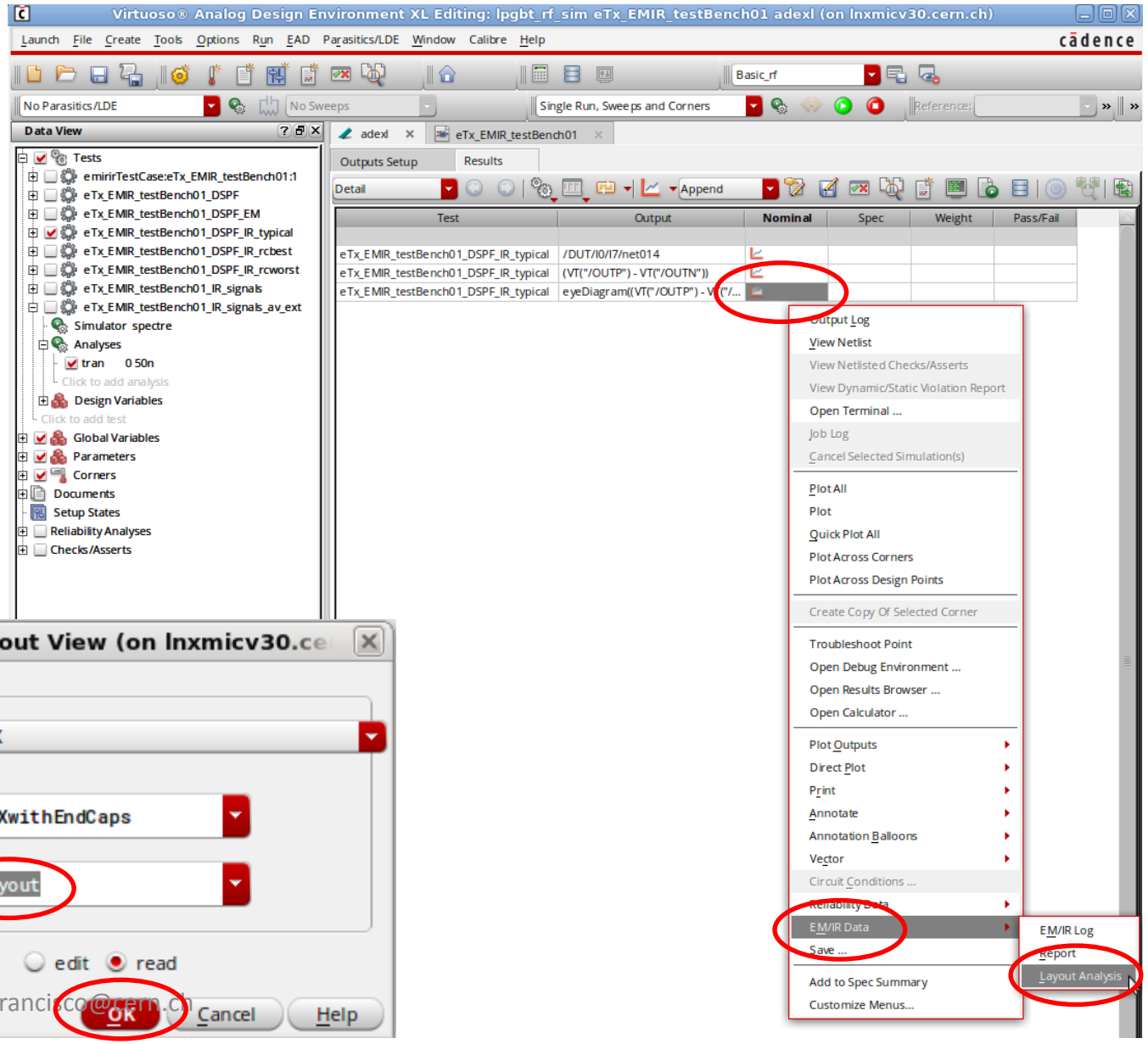
# EMIR Analysis
# Layout Analysis

- To show the results in the layout, RMB over results in the Results tab, EM/IR Data, Layout Analysis
- Select the cell layout view
- Click “OK”





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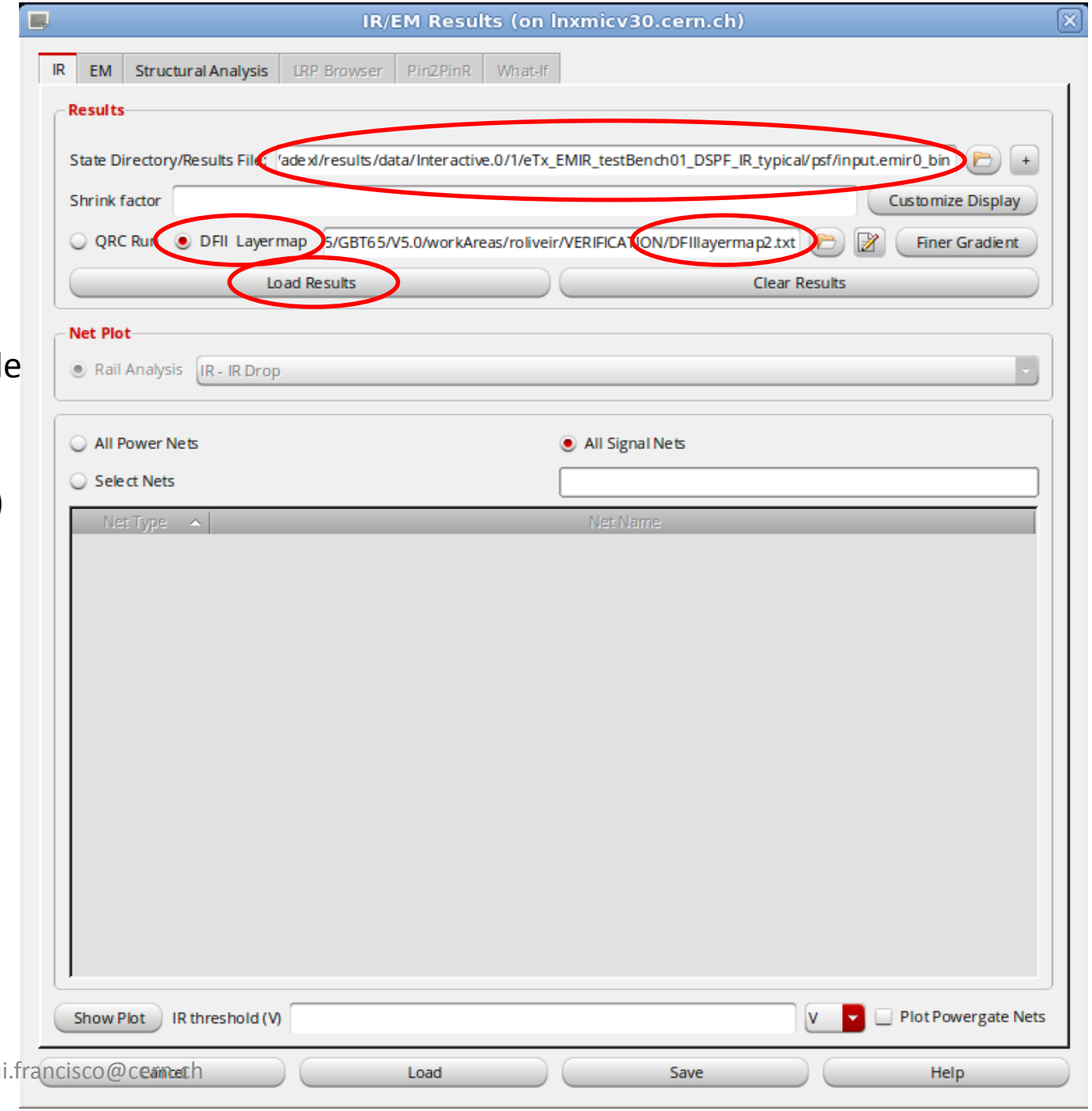
# EMIR Analysis
# IR - Load Results

- Browse for and Select the “input.emir0_bin” file in the simulation results folder
    - /(simulation path)/ResDir/ (design library) /(cell name) /adexl/results/data /(Interactive name)/1/ (test name) /psf/input.emir0_bin
- Select DFII Layermap
- Browse for and Select DFII layermap file
- Click “Load Results”





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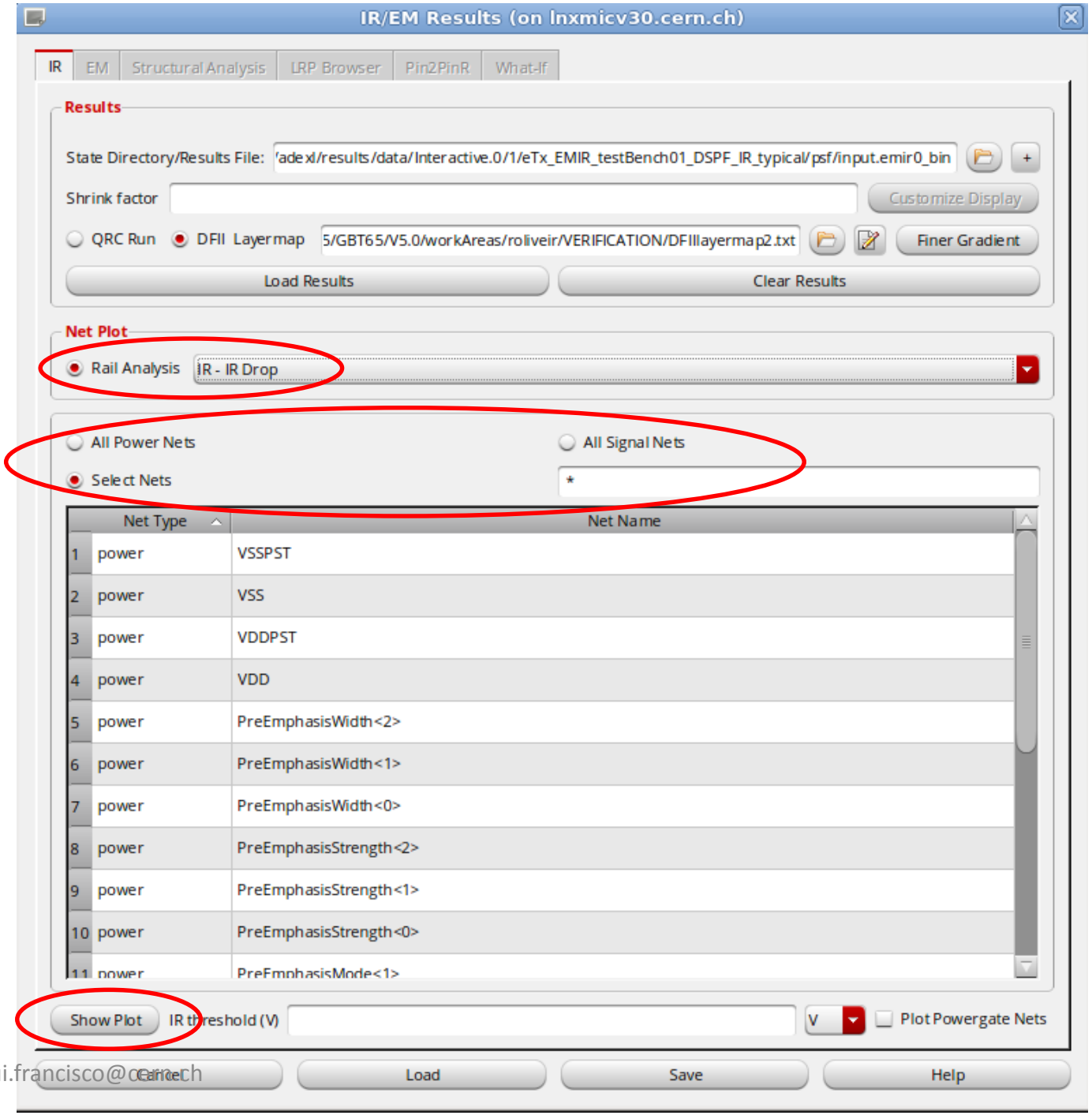
# EMIR Analysis
# IR - Rail Analysis

- Choose Rail Analysis type
  - IR - IR Drop :peak values
  - IRAVG - IR Avg Drop: average values
- Select Nets and/or type of Nets
- Click “Show Plot”





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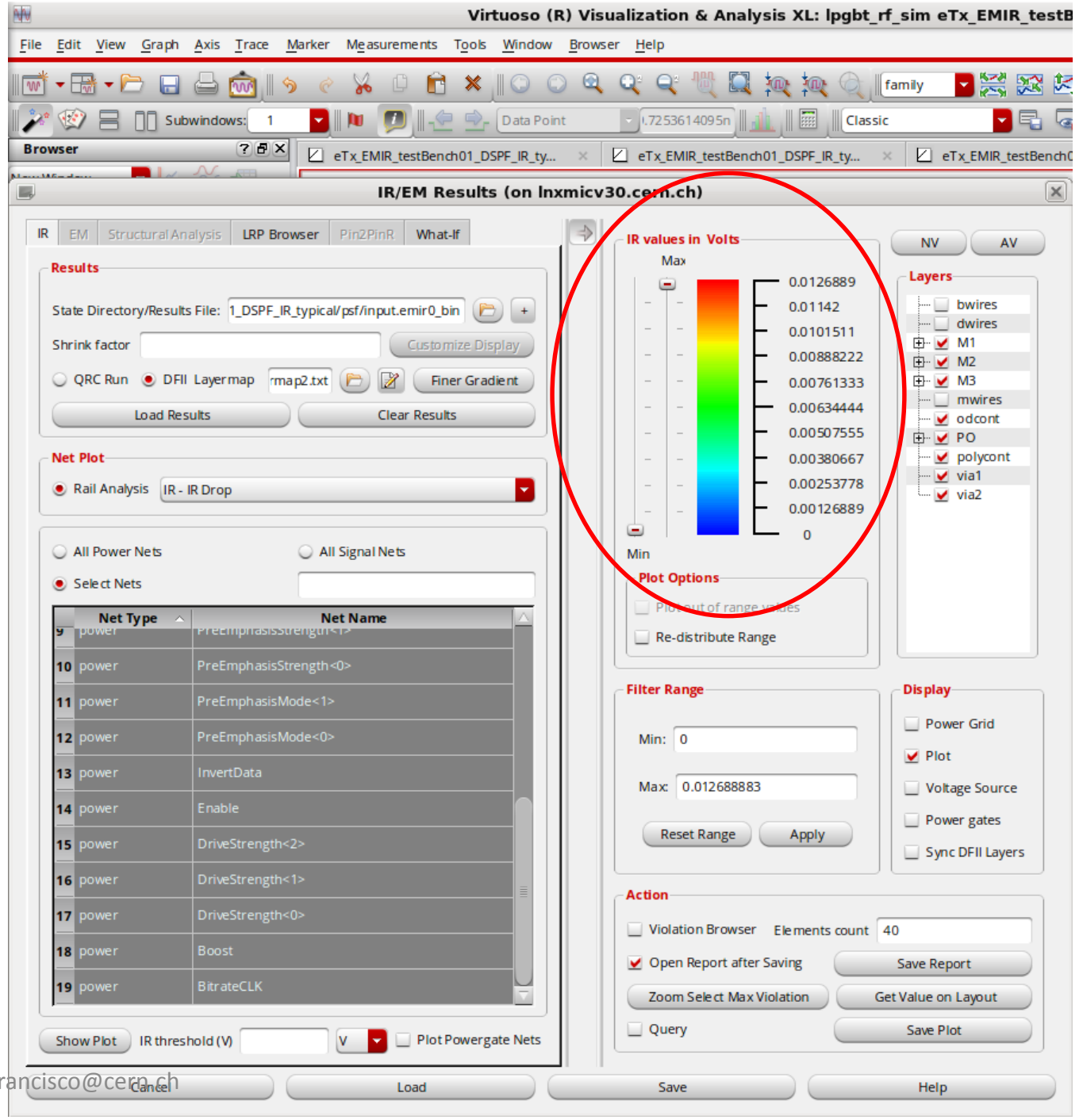
# EMIR Analysis
# IR - Power Nets

- “IR values in Volts” shows the voltage drop scale
- The “Action” panel can be used to find violations / maximum values





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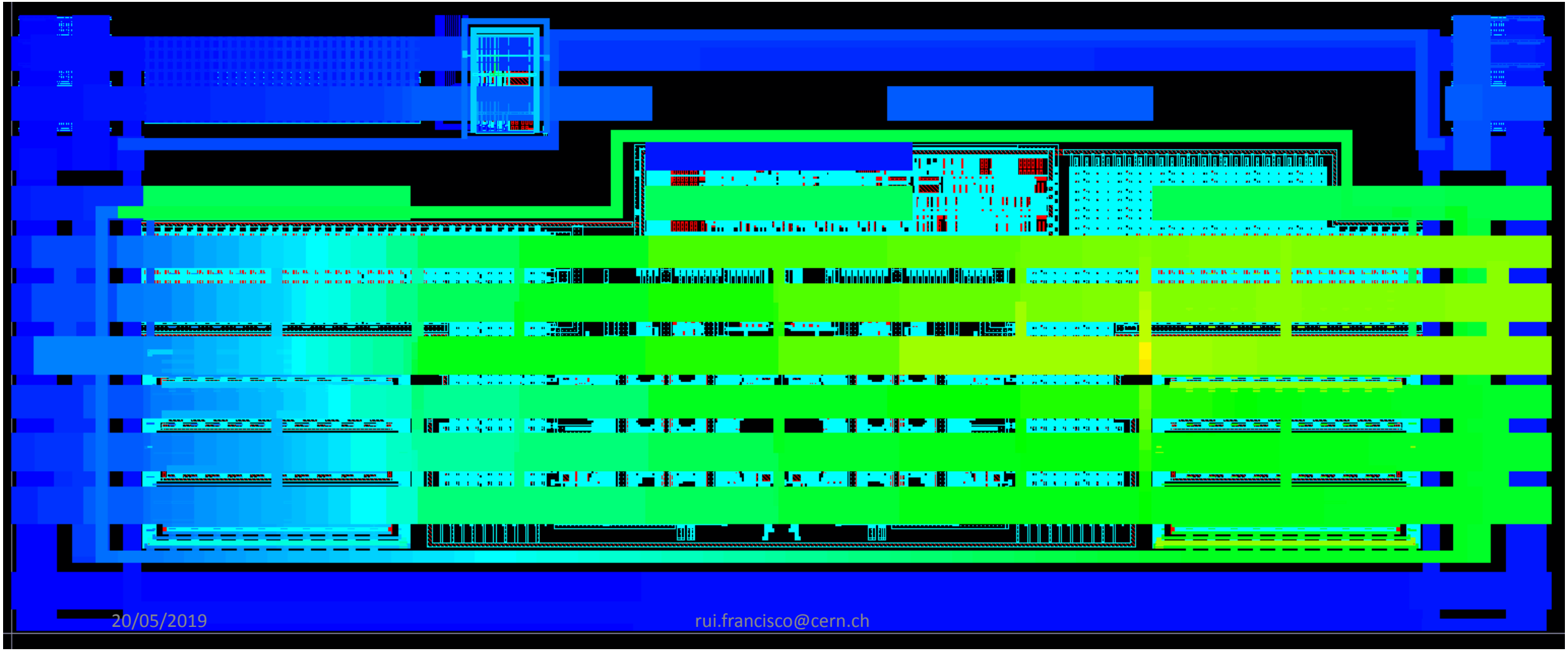
# EMIR Analysis
# IR - Power Nets

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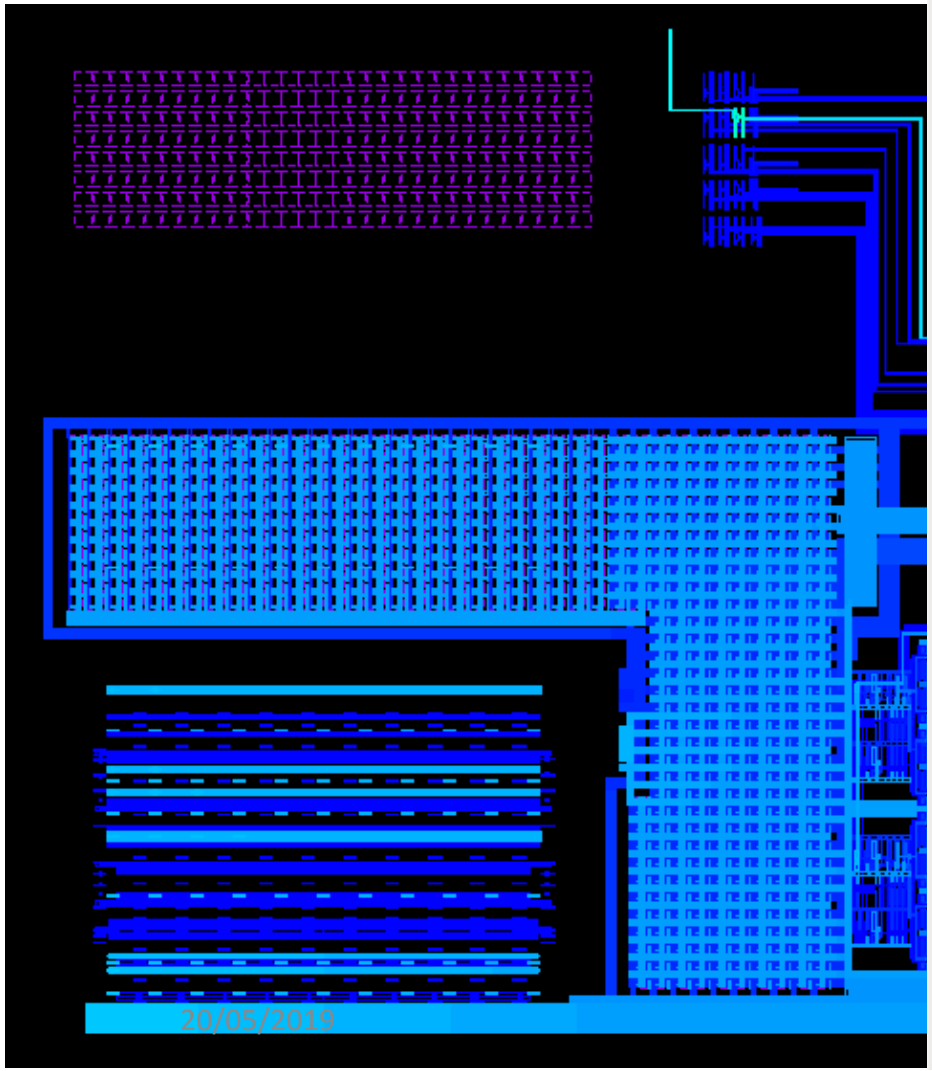
# EMIR Analysis
# IR - Signal Nets




IR/EM Results (on lnxmicv30.cern.ch)

IR | EM | Structural Analysis | LRP Browser | Pin2PinR | What-If

**Results**

State Directory/Results File: 1_DSPF_IR_typical/psf/input.emir0_bin

Shrink factor

Customize Display

QRC Run | DFII Layermap rmap2.txt | Finer Gradient

Load Results | Clear Results

**Net Plot**

Rail Analysis: IR - IR Drop

All Power Nets | All Signal Nets

Select Nets

| | Net Type | Net Name |
|---|---|---|
| 767 | signal | XI0/XI5/XI0/DOWNN<2> |
| 768 | signal | XI0/XI5/XI0/DOWNN<1> |
| 769 | signal | XI0/XI5/XI0/DOWNN<0> |
| 770 | signal | XI0/XI2/N3 |
| 771 | signal | XI0/XI2/N2 |
| 772 | signal | XI0/XI2/N1 |
| 773 | signal | XI0/VSSPSTint |
| 774 | signal | XI0/VDDPSTint |
| 775 | signal | OUTP |
| 776 | signal | OUTN |
| 777 | signal | Data |

Show Plot | IR threshold (V) | V | Plot Powergate Nets

**IR values in Volts**

Max 0.166208 | 0.149588 | 0.132967 | 0.116346 | 0.0997253 | 0.0831045 | 0.0664838 | 0.049863 | 0.0332422 | 0.0166215 | 7.16405e-07 Min

NV | AV

**Layers**

bwires | dwires | M1 | M2 | M3 | mwires | odcont | PO | polycont | via1 | via2

**Plot Options**

Plot out of range values

Re-distribute Range

**Filter Range**

Min: 7.164046e-07

Max: 0.16620837

Reset Range | Apply

**Display**

Power Grid | Plot | Voltage Source | Power gates | Sync DFII Layers

**Action**

Violation Browser | Elements count 40

Open Report after Saving | Save Report

Zoom Select Max Violation | Get Value on Layout

Query | Save Plot

Cancel | Load | Save | Help

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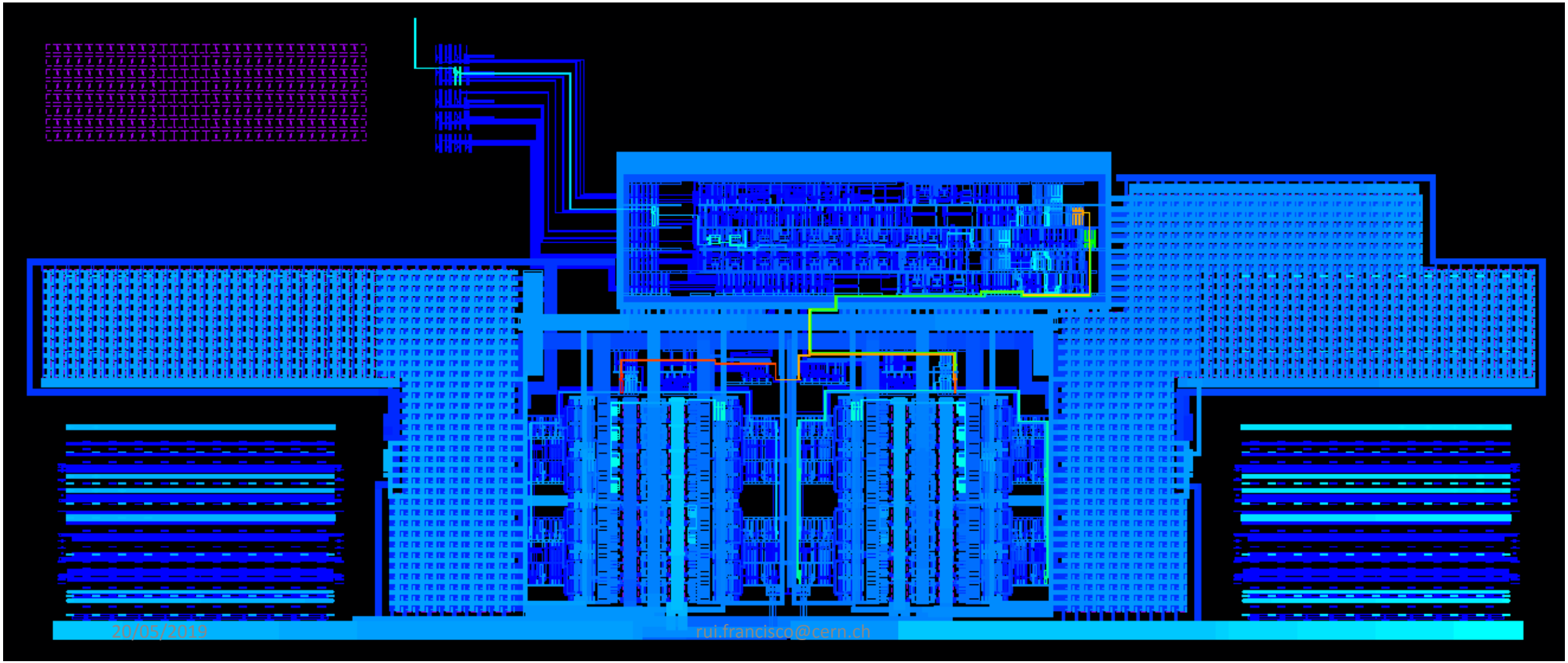
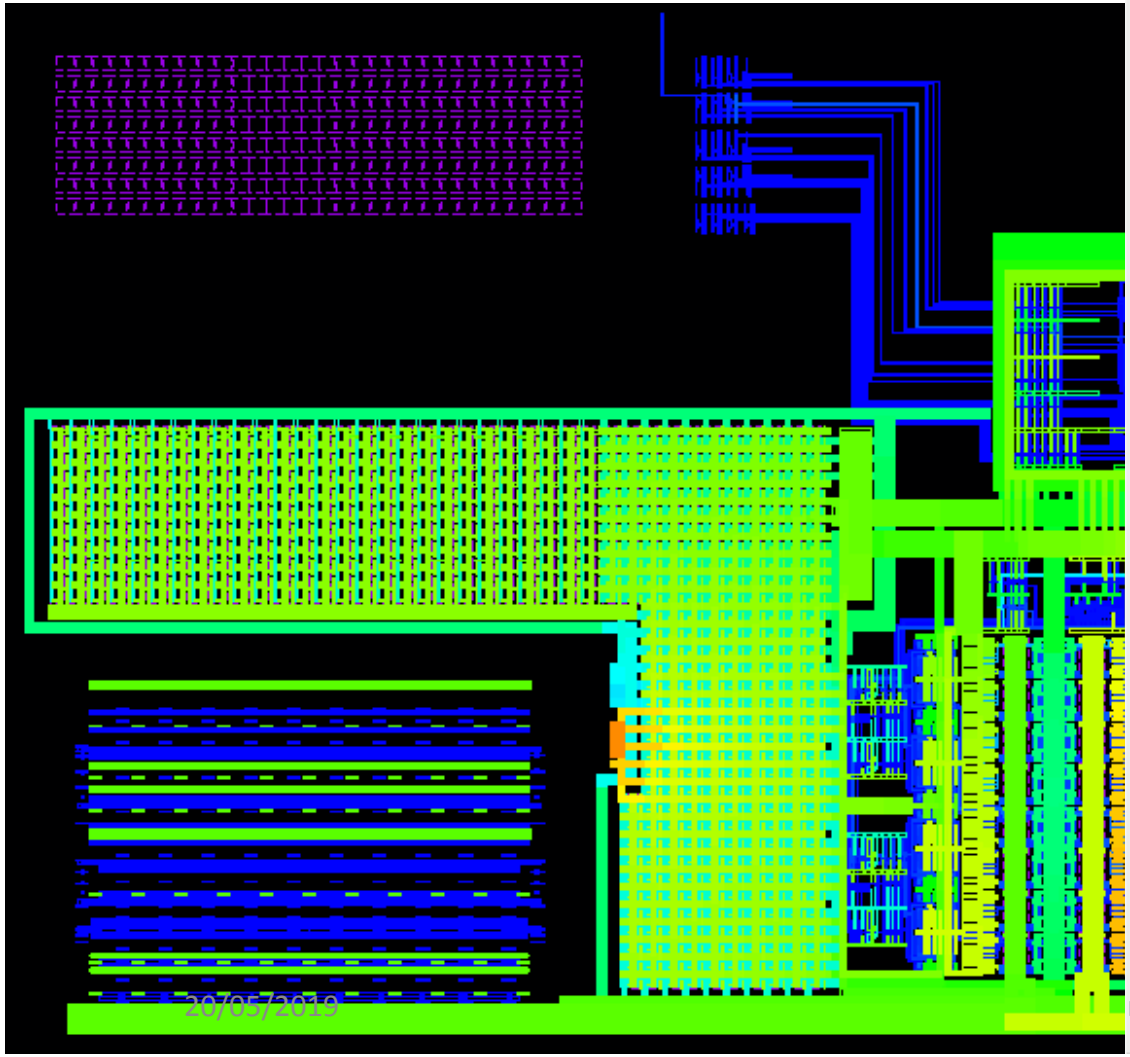
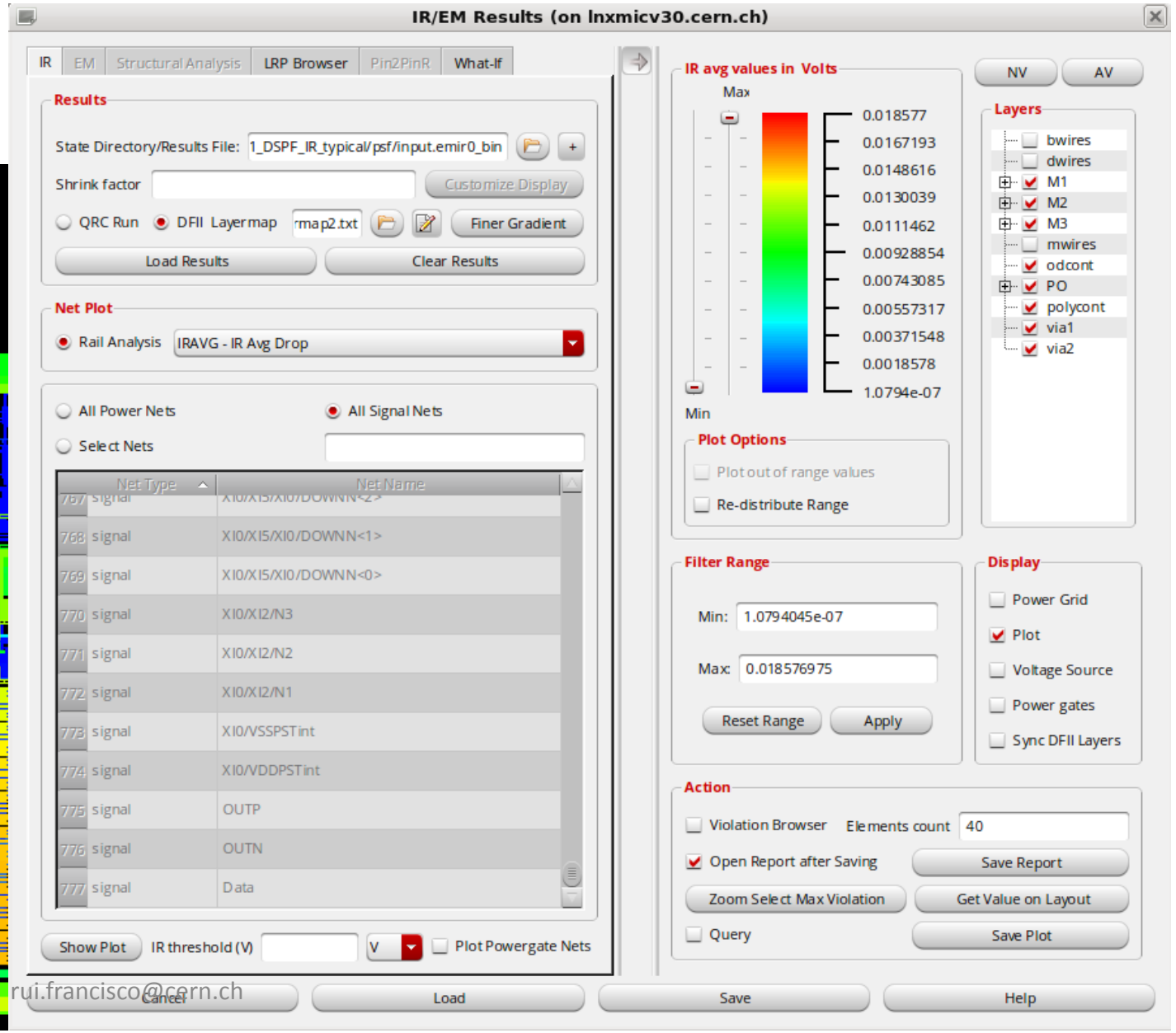
# EMIR Analysis
# IR - Signal Nets



# EMIR Analysis
# IR AVG - Signal Nets







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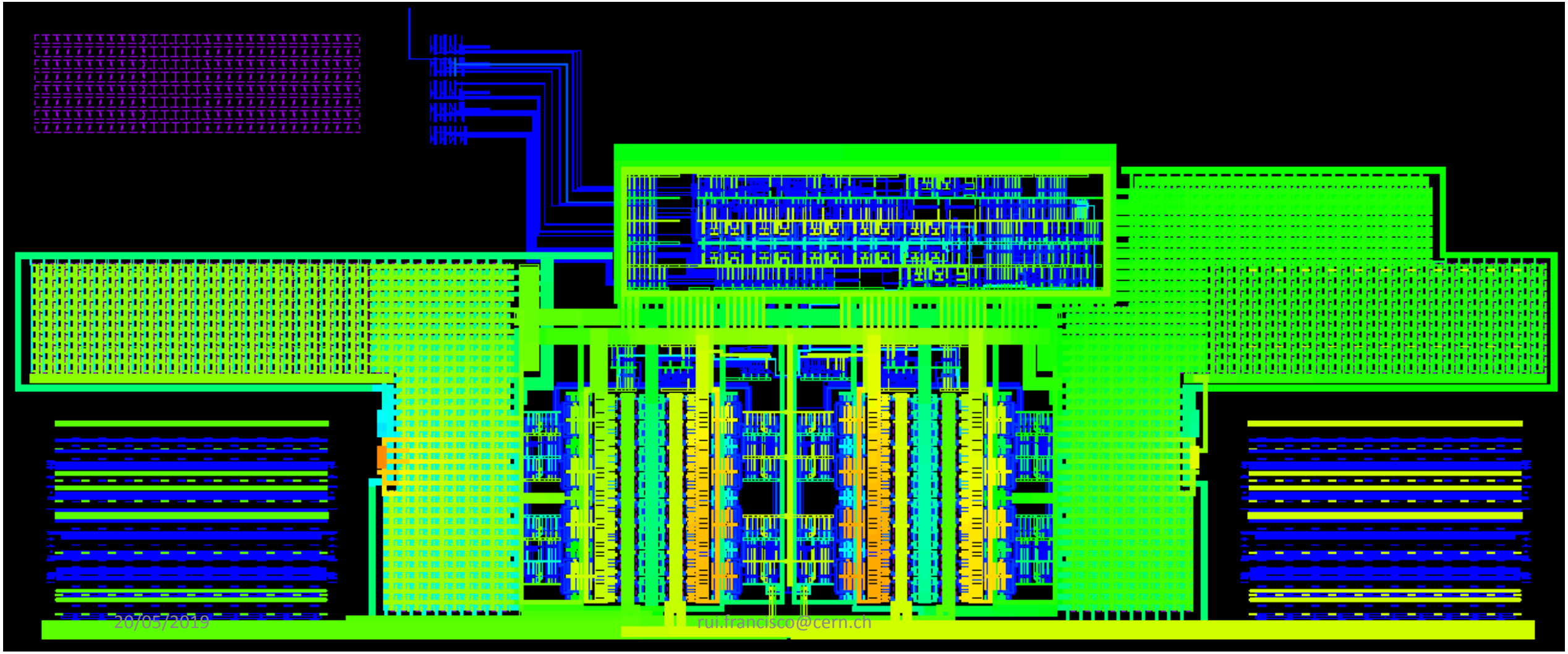
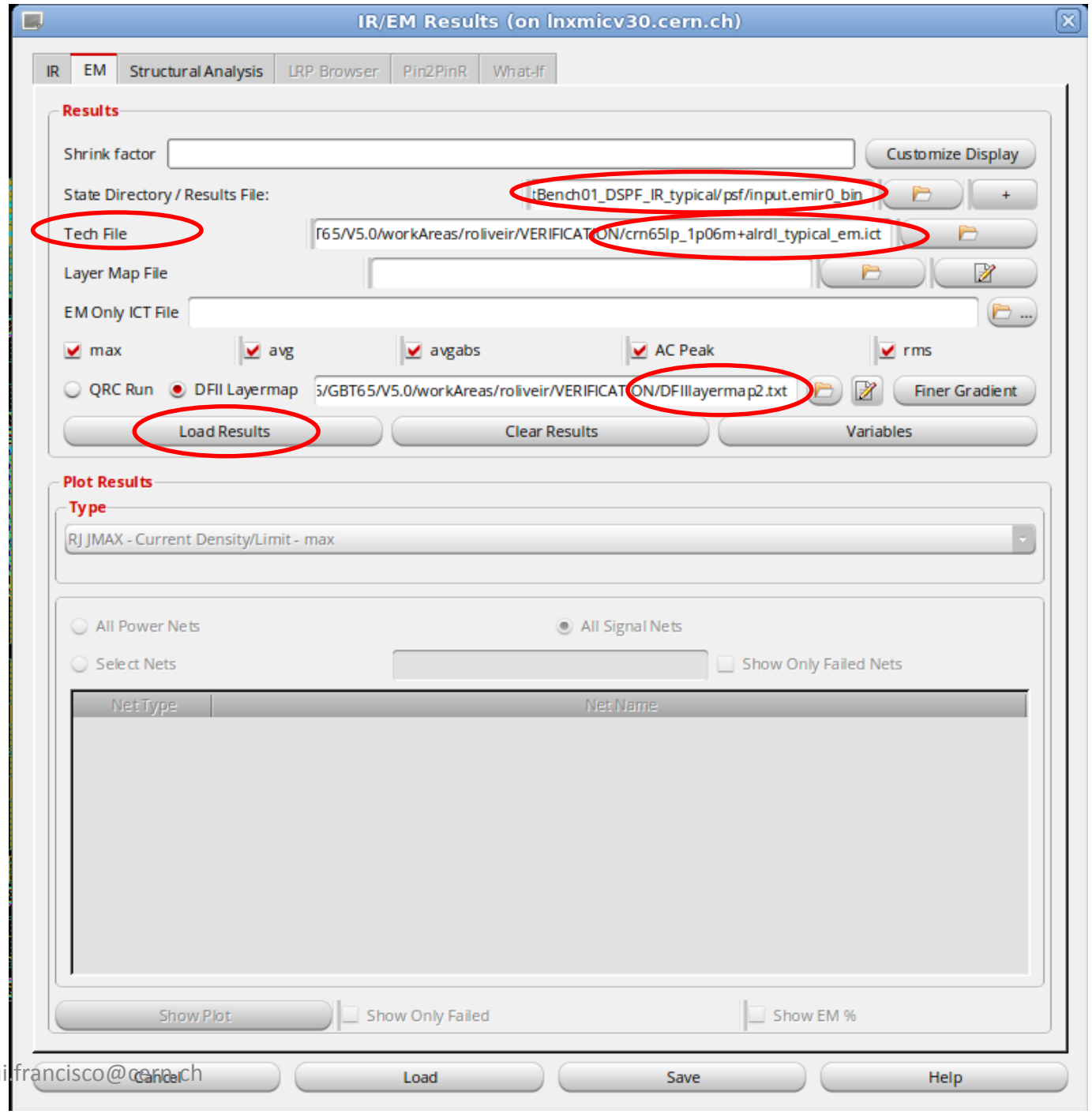
# EMIR Analysis
# IR AVG - Signal Nets



# EMIR Analysis
# EM - Load Results

- Browse for and Select the “input.emir0_bin” file in the simulation results folder
    - /(simulation path)/ResDir/ (design library) /(cell name) /adexl/results/data /(Interactive name)/1/ (test name) /psf/input.emir0_bin
- Add the previously used “*_em.ict” Tech File
- Select DFII Layermap
- Browse for and Select DFII layermap file
- Click “Load Results”





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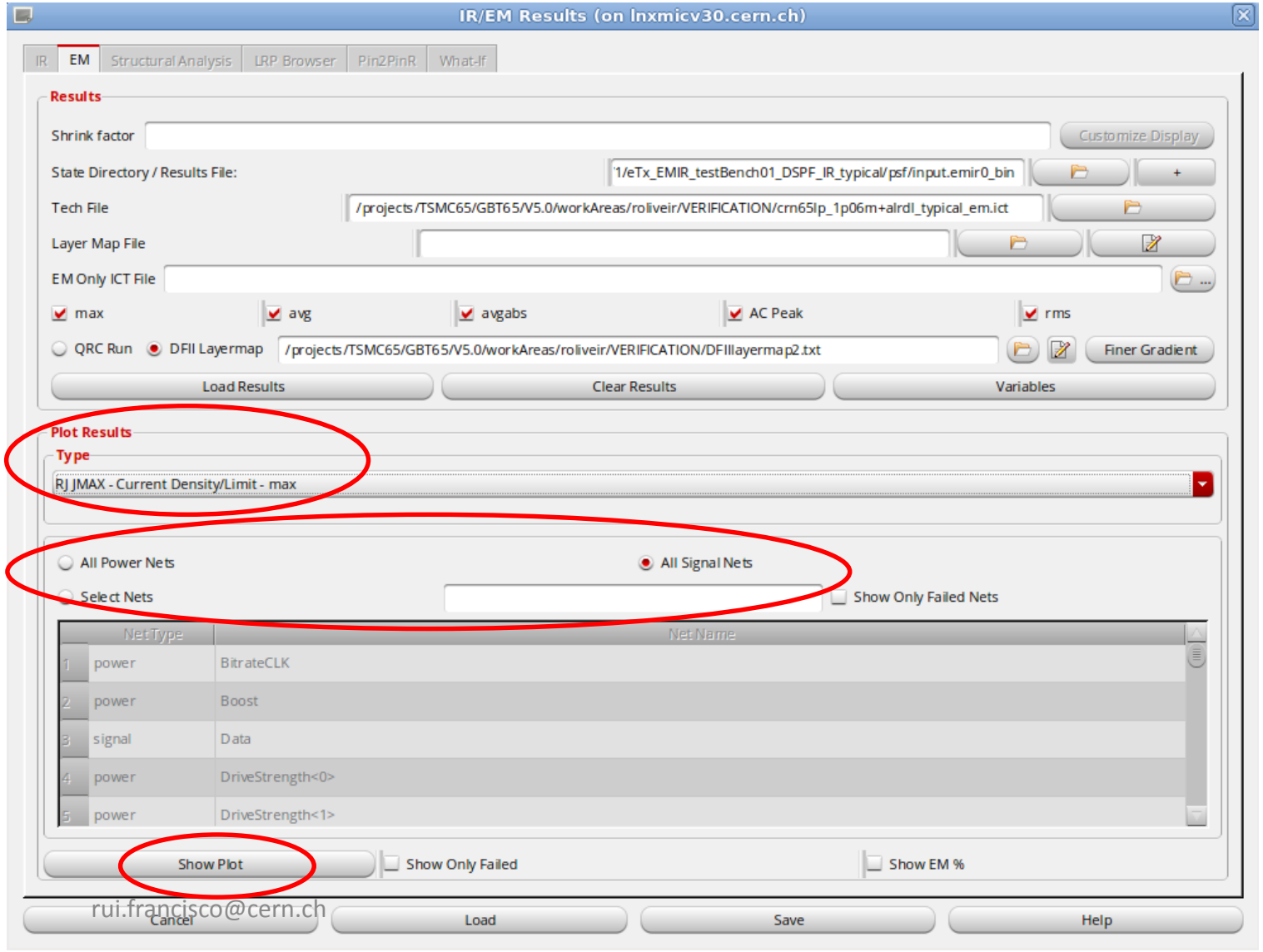
# EMIR Analysis
# EM - Type

- Choose Plot Results type
  - RJ JMAX - Current Density / Limit
- Select Nets and/or type of Nets
- Click “Show Plot”





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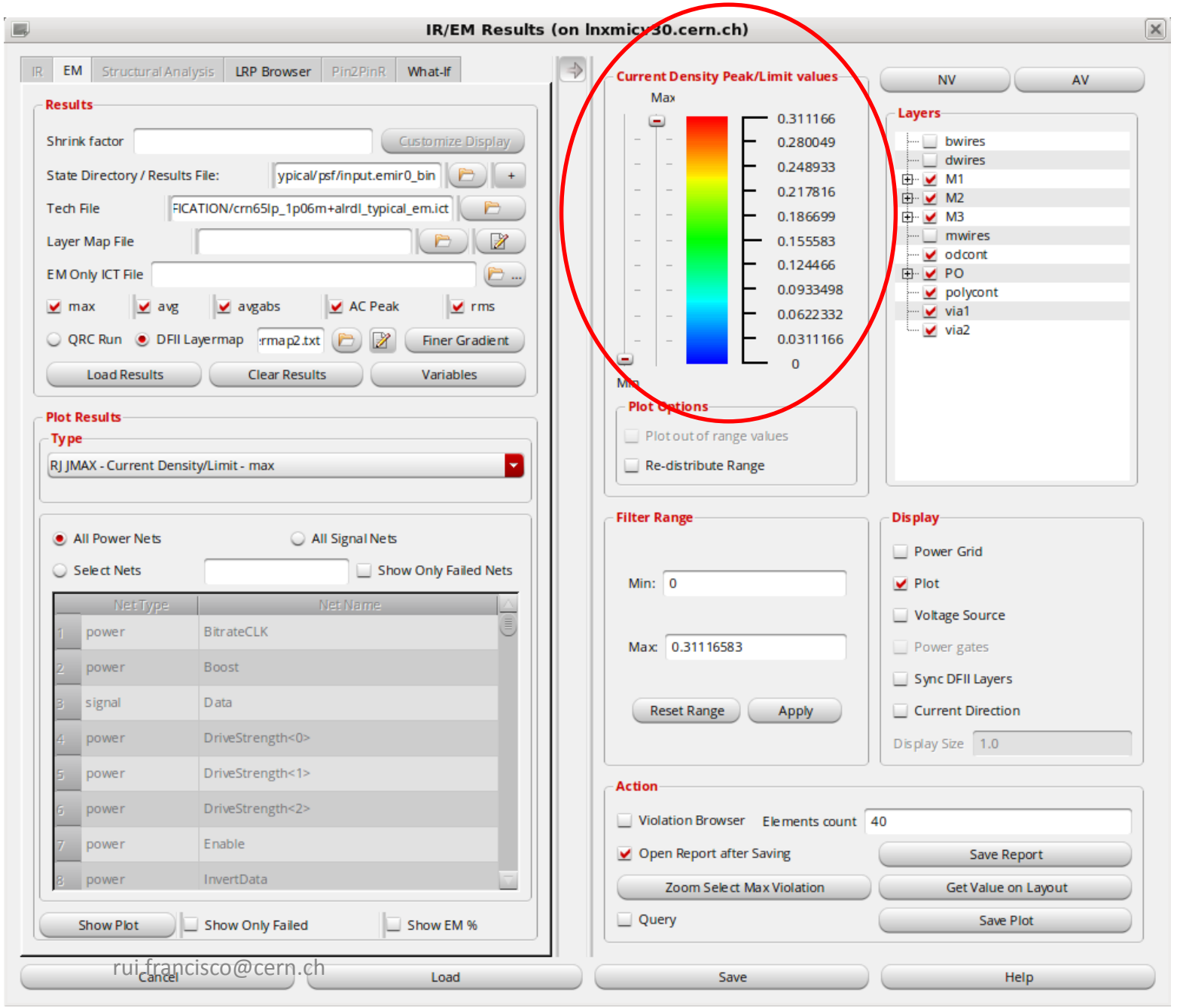
# EMIR Analysis
# EM - Power Nets

- "Current Density Peak/Limit values" shows the ratio of current capability used
- In this example 31% of the path current capability is being used
- The "Action" panel can be used to find violations / maximum values
- If selecting the "Show EM %", the "Save Report" can show false failing situations due to a bug in current density calculation





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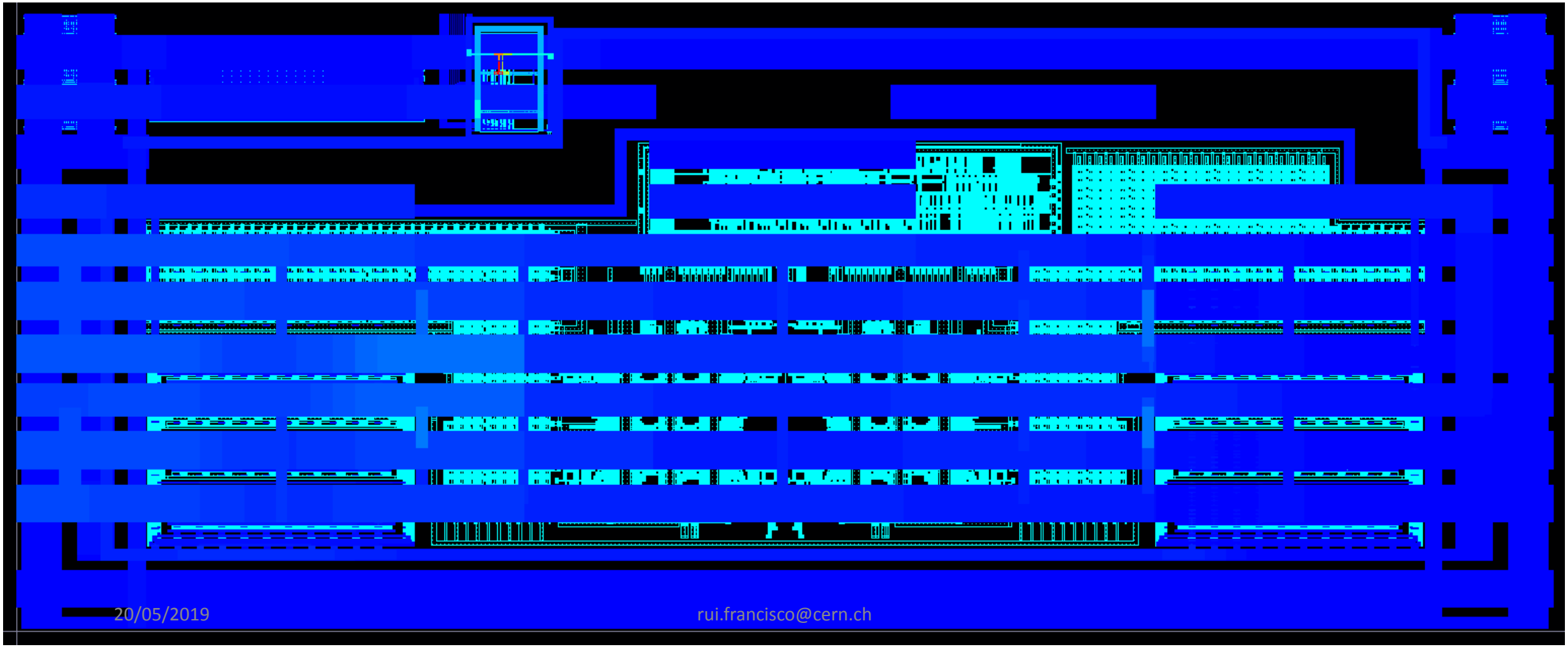
# EMIR Analysis
# EM - Power Nets

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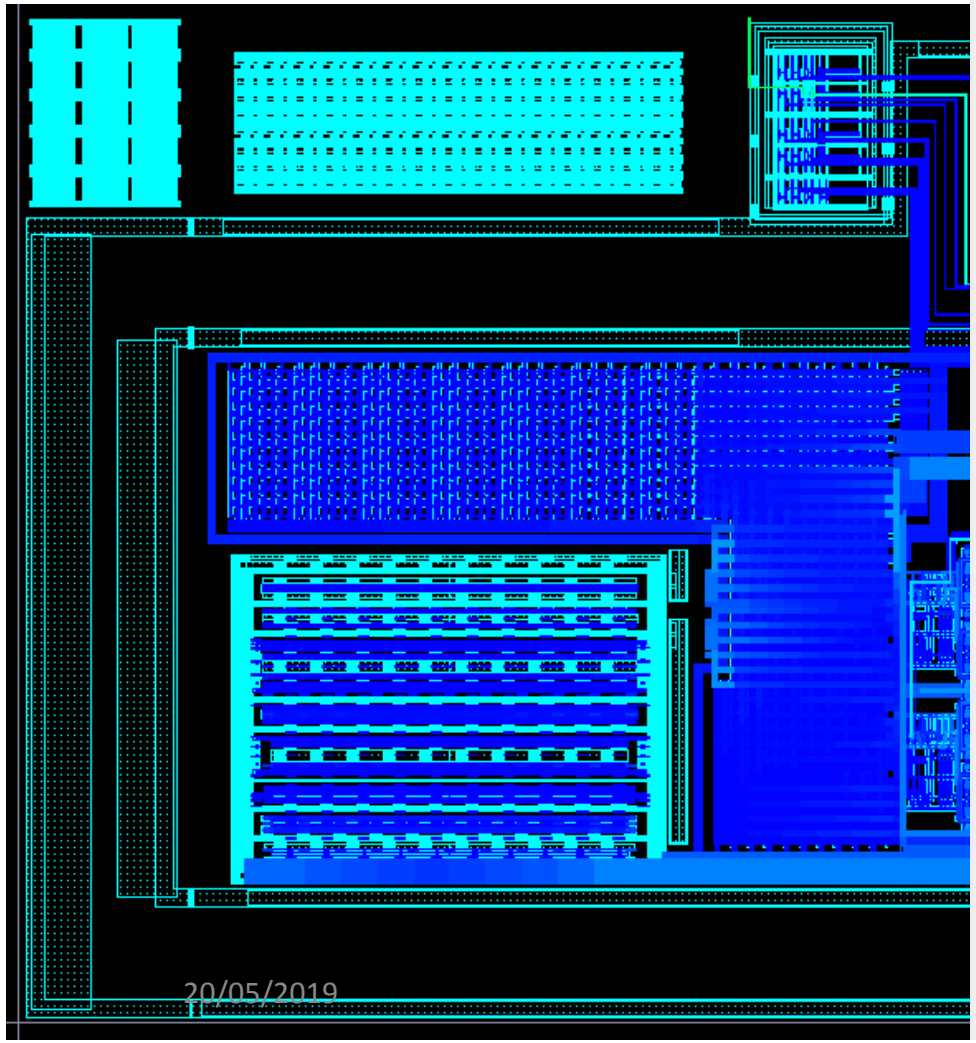
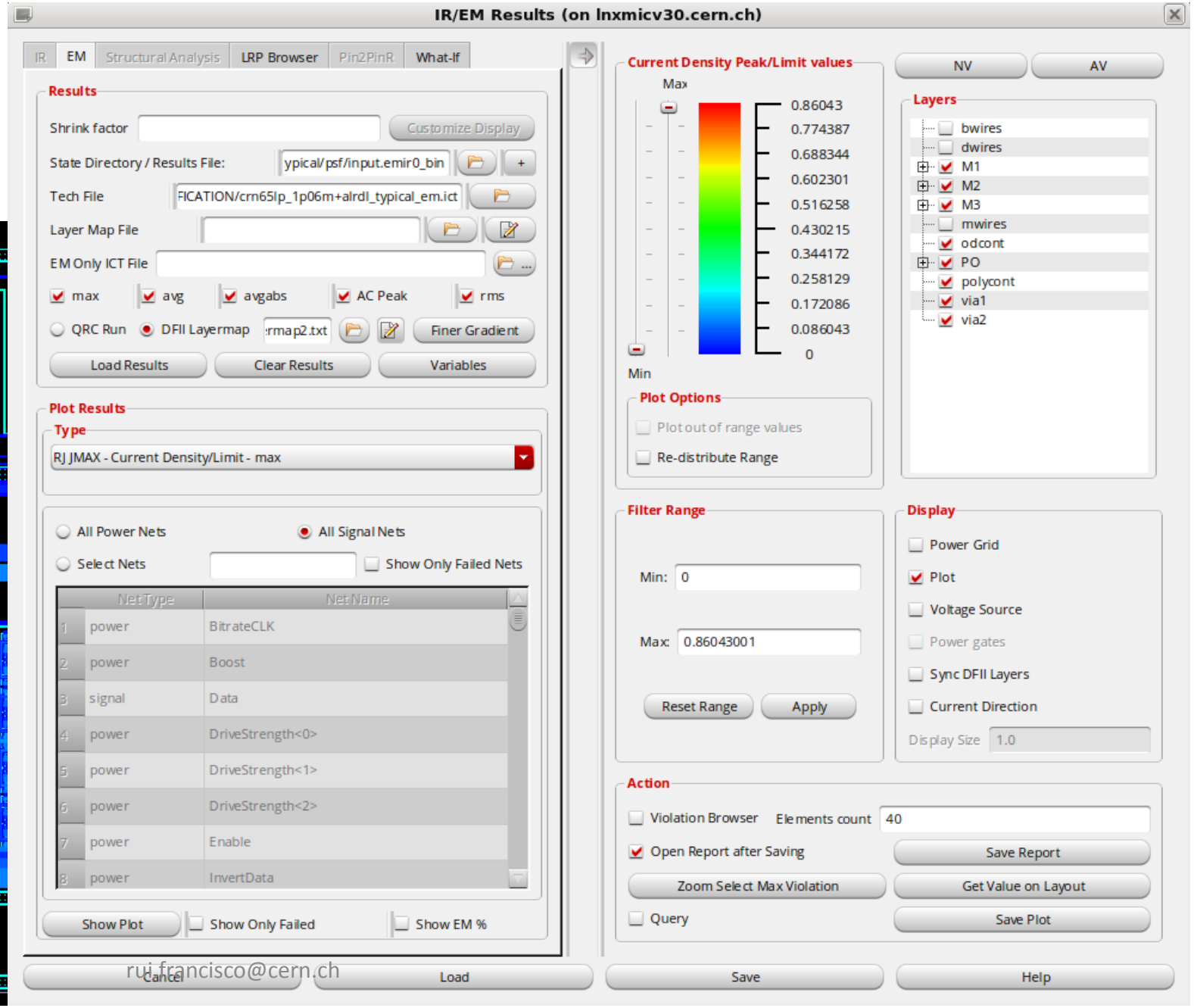
# EMIR Analysis
# EM - Signal Nets







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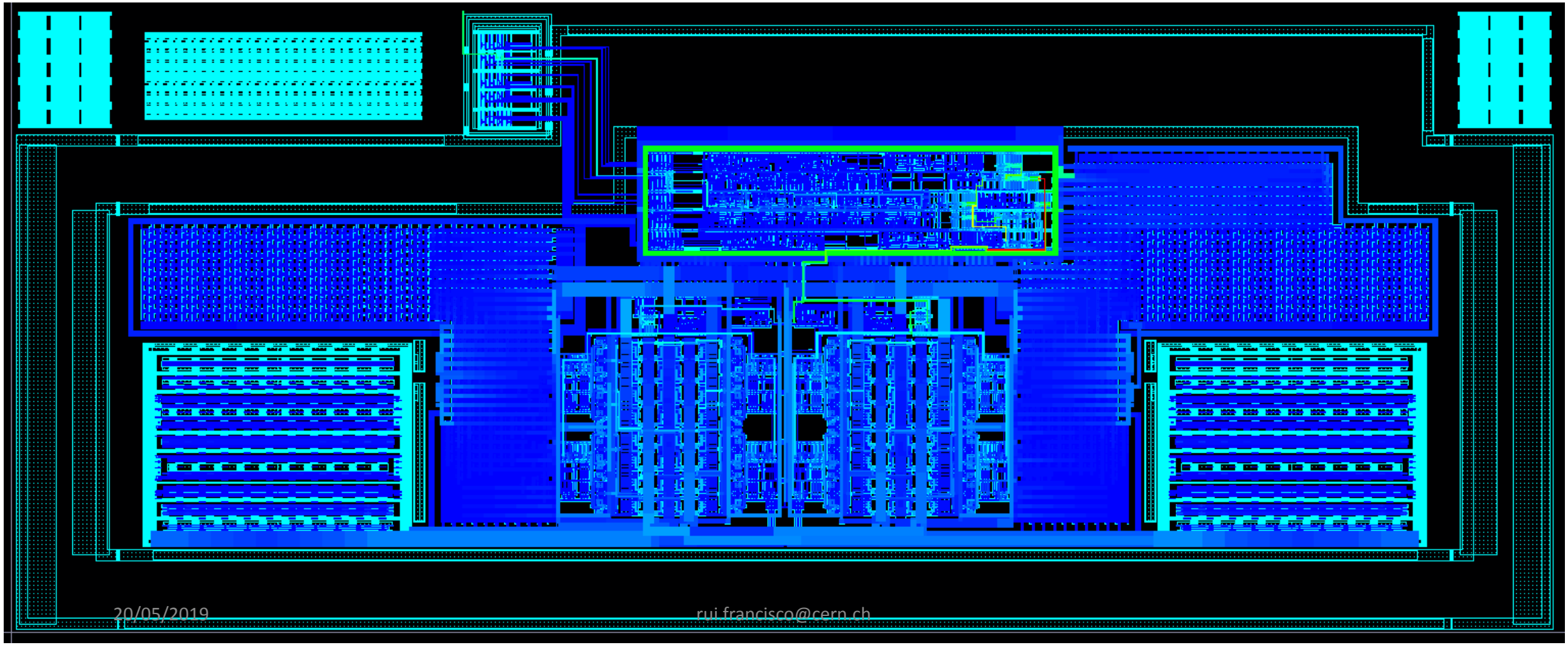
# EMIR Analysis
# EM - Signal Nets



# The End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# APPENDIX

# pvtech.lib

-- DEFINE  tsmc65n $PDK_PATH/V1.7A_1/$OPTION/PVS_QRC

DEFINE tsmc65n ./PVS_QRC

# crn65lp_1p06m+alrdl_typical_em.ict

```
#####################################################
#####  ICT File Generated by ircxtoict -em_update
#####  ircxtoict Release : 15.2.1-s070
#####  IRCXTOICT Control ID : 2.52
#####  Input IRCX File : RC_IRCX_CLN65LP_1P6M+ALRDL_3X2Z_typical.ircx
#####  Input IRCX File version : V1.5a #####  Input ICT File : crn65lp_1p06m+alrdl_typical.ict
#####  Output ICT File : crn65lp_1p06m+alrdl_typical_em.ict
#####################################################
process "crn65lp_1p06m+alrdl_typical" {
…
```


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# DFIIlayermap2.txt

#<type> <extraction_layer_name> <dfII_layer_name>

| | | |
|---|---|---|
| metal | metal1 | M1 |
| metal | metal2 | M2 |
| metal | metal3 | M3 |
| metal | metal4 | M4 |
| metal | metal5 | M5 |
| metal | metal6 | M6 |
| metal | metal7 | AP |
| poly | poly | PO |
| od | od | OD |
| via | odCont | CO |
| via | via1 | VIA1 |
| via | via2 | VIA2 |
| via | via3 | VIA3 |
| via | via4 | VIA4 |
| via | via5 | VIA5 |
| via | via6 | RV |

# rnpolys_sub_circuit.spi

- ++++++++++++++++++++++++++++++++++++++++++++++++++++++++++ *
- * Sub cell: rnpolys *
- * ++++++++++++++++++++++++++++++++++++++++++++++++++++++++++ *
- .subckt rnpolys PLUS MINUS
- .ends rnpolys

# References


- IC6.1.7: Voltus-Fi EMIR Analysis Workshop- The DSPF flow:

  https://support.cadence.com/apex/articleattachmentportal?id=a1O0V000009ETFdUAO&pageName=ArticleContent&attachId=0690V000004Z7ypQAC&sq=null

- Voltus-Fi-L EMIR Analysis Workshop - Extracted View Flow:

  https://support.cadence.com/apex/ArticleAttachmentPortal?id=a1O0V000007MnylUAC&pageName=ArticleContent

- EM models from Cadence support how to:

  https://community.cadence.com/cadence_blogs_8/b/di/posts/five-minute-tutorial-creating-an-em-model-file

  https://community.cadence.com/cadence_blogs_8/b/di/posts/five-minute-tutorial-em-model-files-revisited

  https://community.cadence.com/cadence_blogs_8/b/di/posts/five-minute-tutorial-one-more-look-at-em-models